Preliminary design of readout electronics for the Mimosa pixel sensors of Alice Forward Calorimeter

1. Hardware

1.1 System Diagram

For the upcoming beam test of Mimosa CMOS pixel detector(Mimosa23/Phase1[1]), As in figure1, there will be a minitower with a sandwich structure made up of 24 tungsten and silicon layers and on every silicon layer there are 4 Mimosa pixel sensors. Seven 8-core twist pair cables connected to RJ45 sockets on the readout electronics are necessary for the readout of these 4 detectors: 4 cables for data output of 4 sensors, 1 for JTAG, 1 for Clock and Control, and 1 for chip reset signal RSTB and signal ground, the last 3 cables are shared between the 4 sensors within one layer. The distance between detector minitower and readout electronics will be less than 10 meters. Scintillator plates are used for the generation of trigger signals which will be sent to FPGAs to control the readout procedure. Raw data from every pixel detector will be compressed and packaged to be sent out via high speed optical links to a DAQ PC for further processing.

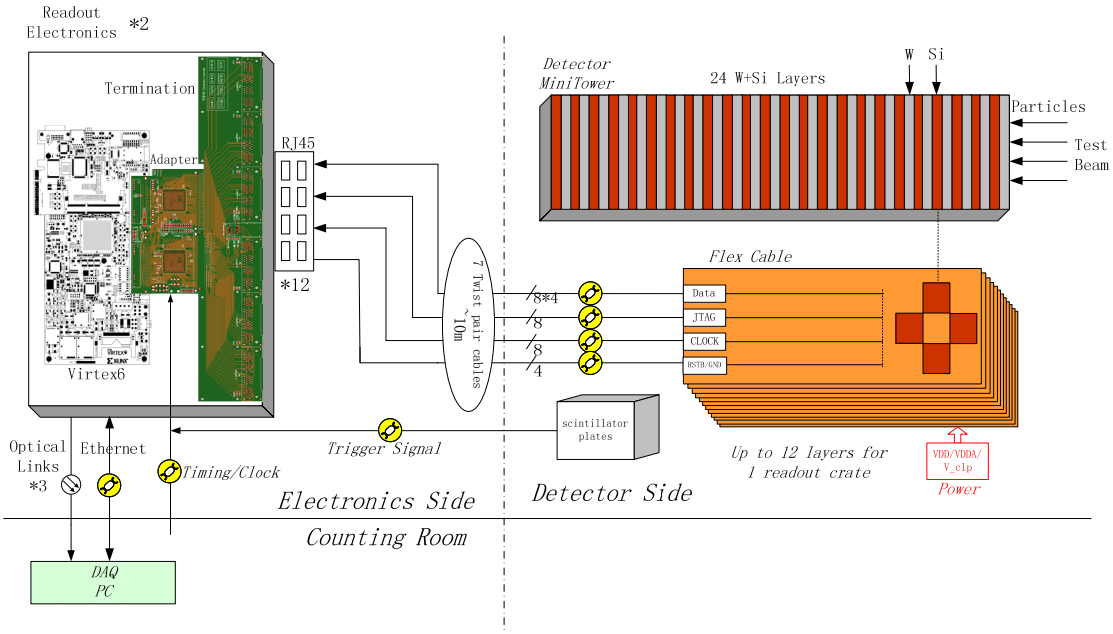

Figure1. System diagram for beam test of Mimosa detector

As described in Figure2, 12 layers of sensors (48 Mimosas) can be read out by one set of electronics, which consists of a Virtex6 FPGA DEV board[2], an Adapter board[3] equipped with 2 Spartan6[4] FPGAs connecting to Virtex6 FPGA board via two FMC connectors, and two Termination boards[3] with 6 RJ45 modular jacks on each used for the distribution of signal links via twist cables to 24 Mimosa sensors, two 500pin FMC connectors are used between the adapter board and the termination boards, with one of them being on the top layer(red) and the other on the bottom layer(blue) of the Adapter board.

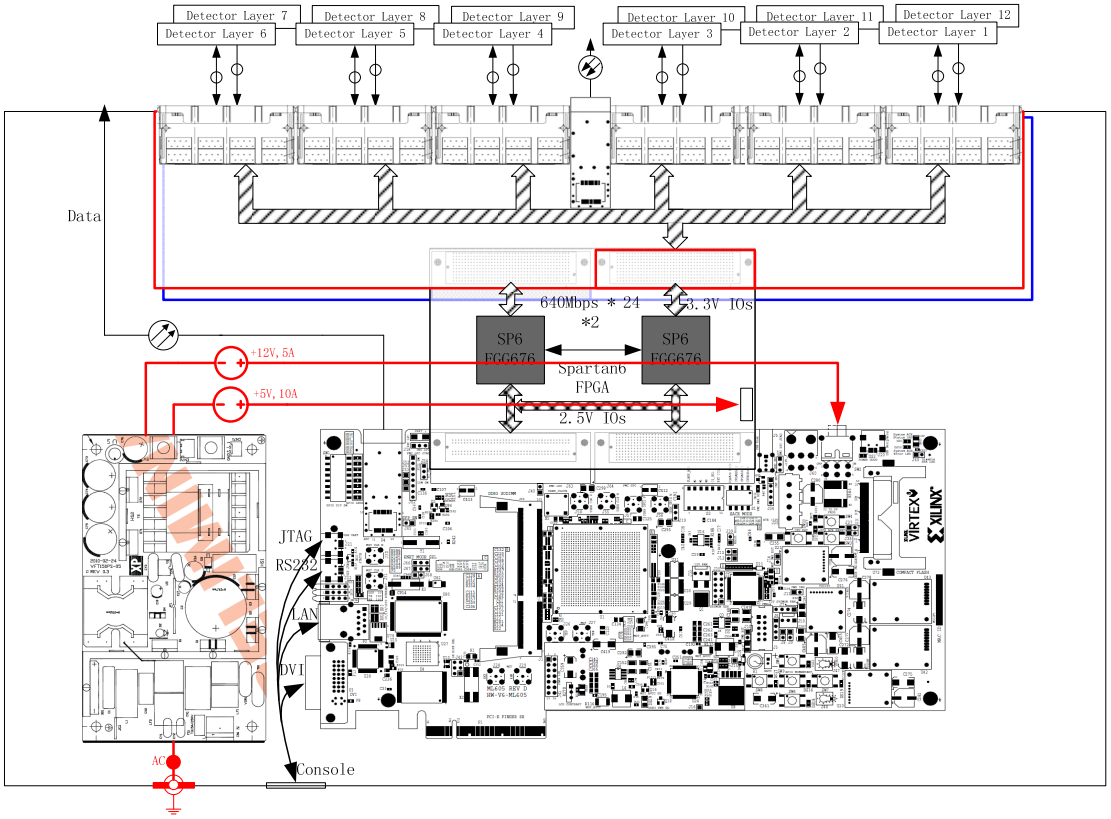

Figure2. System diagram of readout electronics

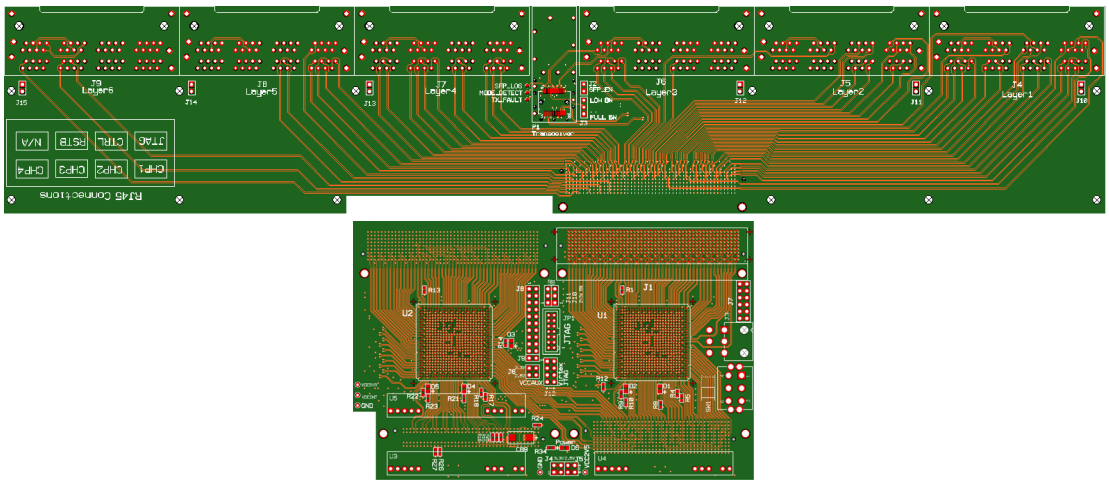

Figure3. Layout of Adapter and Termination board

Figure3 gives the layout of the Adapter board and the Termination board. Six two-layer stacked RJ45 connectors(each for one detector layer) are used to save space on the Termination board, there is also another optical link on every termination board dedicated for data output which utilizes the MGT transceiver from Virtex6 DEV board, so there will be 3 optical links in all for 48 Mimosa sensors. The Termination boards on the top and bottom layer of the Adapter board are interchangeable based on the symmetric floor plan of optical transceiver, RJ45 connectors and mounting holes. As for the Adapter board, two Spartan6 FPGAs are firstly used as level shifters between 2.5V and 3.3V IOs because the latter one is not supported by Virtex6, also only with the

help of Spartan6, enough IOs are available for the connections to up to 48 Mimosa sensors for one Virtex6 DEV board, and Spartan6 gives the ability for the first level data sparsification to reduce the incoming data rate for Virtex6 FPGA. There are 16 spare signal links between these two Spartan6 FPGAs which may play the role of synchronization/communication, also necessary Timing/Trigger/Control signals could be sent to Spartan6 or Virtex6 with these spare IO connections.

1.2 Signal Connections

Figure 4 shows the signal connections between Mimosa sensors and readout electronics. For every Mimosa chip, besides the analog/digital and Vclp power supply, there are 4 LVDS data output signals which are mandatory, 4 single ended JTAG signals for configurations and an RSTB as the global reset input of Mimosa chip, an LVDS master clock input(CKR), two LVDS output signals(Marker) concerning readout timing/synchronization of digital data, and two single ended control signals, START for synchronizing the outputs, and SPEAK (which is only for analog readout, N/A in our case). To ensure the signal quality after long distance transmission, all of the above signals will be in LVDS between detector Minitower and readout electronics.

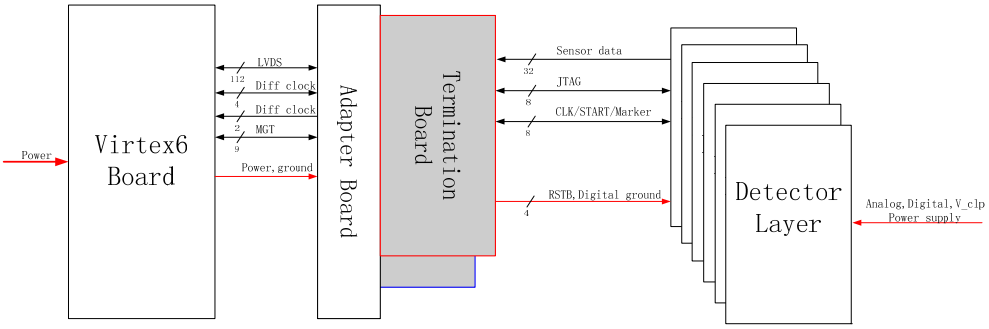

Figure4. Signal Connections between detectors and readout electronics

From the detector side view, for a detector layer with 4 Mimosa sensors, as illustrated in Figure5, only one JTAG interface is needed if all the 4 sensors are daisy chained; also for the clock and control signals, CKR/START input could be shared by all the 4 detectors within one layer, the Marker (MK_CLKD) and clock return (CLKD) output signals should be connected only to one of the 4 Mimosa sensors.

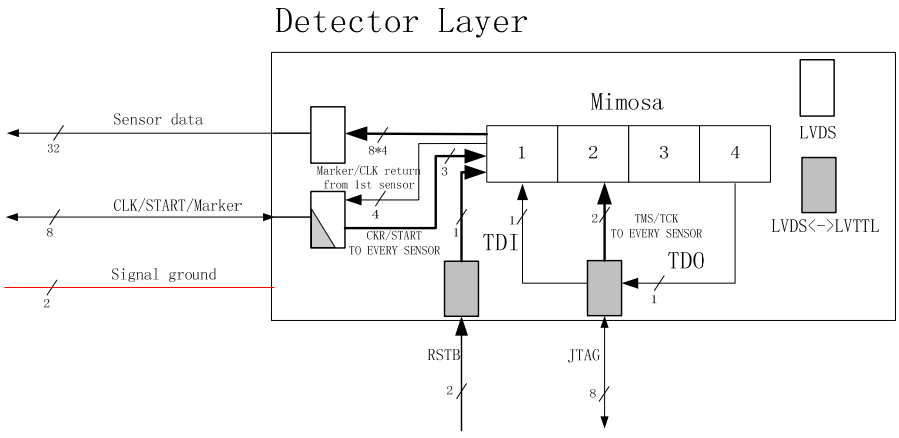

Figure5. Signal Connections for a detector layer with 4 Mimosa sensors

All these signals from a detector layer need to be connected to 7 RJ45 connectors on the readout electronics with 50ohm twist cables. Figure6 shows the signal connections at the readout electronics side, arrow represents the signal direction for Spartan6 which is contrary at the detector side. TDI/TDO in JTAG connector corresponds to the TDI/TDO pin of Mimosa sensor, with TDI as signal output and TDO as signal input for Spartan6; besides the RSTB and signal ground (connected in series with a 0 ohm resistor or a ferrite bead for grounding configuration), there are two spare LVDS25 signals in the 7th RJ45 connector which may be used for every detector layer as backup connections or for future applications such as control of an I2C bus ADC for temperature/voltage/current monitoring.

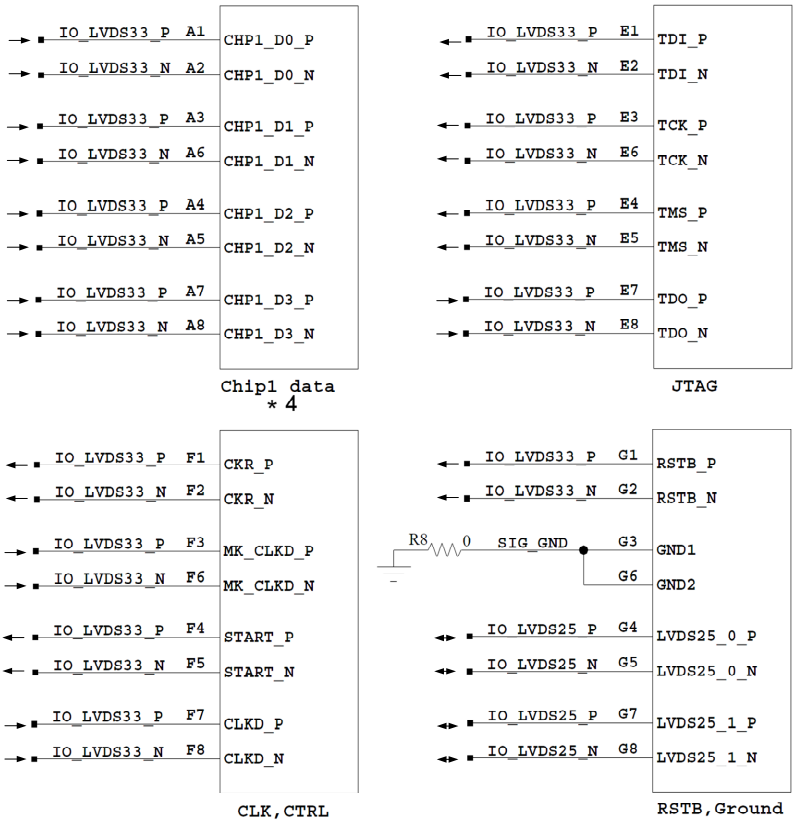

Figure6. RJ45 signal connections in LVDS pair

Under this circumstance, there should also be a termination board at the detector side to convert some LVDS signals (JTAG/START/RSTB) to LVTTL before applying to Mimosa sensors, of course buffers and other functionalities could also be realized on this termination board.

1.3 Adapter board

The Adapter board is in the middle of Virtex6 DEV board and the Termination board, holding 2 XC6SLX100-FGG676 FPGAs with two 2.5V IO banks connected to Virtex6 and other four 3.3V IO banks connected to the Termination boards.

I/O banks setup

As in figure7, XC6SLX100-FGG676 has 480 user IOs divided into 6 banks which are fully pin-compatible with XC6SLX150-FGG676 except that there are 18 extra IOs in Bank0 for the latter one, all these 6 banks independently can have different IO voltage for the corresponded signal standard but only IOs from bank0 and bank2 could be utilized as differential outputs. Bank2 also contains the multiplexed signals for FPGA configuration and settings, the IO voltage of bank2 is set to 2.5V which makes it possible to connect those signals to Virtex6 DEV board and let Virtex6 take care of the configuration and control of the two Spartan6 FPGAs. There are 112 LVDS pairs plus some other signals available from the two FMC connectors on the Virtex6 DEV board to be distributed to two Spartan6 FPGAs, bank1 is also configured as 2.5V to be connected to Virtex6 together with bank2 for the data transmission between Spartan6 and Virtex6, most of the extra I/O signals from these two banks are assigned as: Spare I/Os, inter-connections between the two Spartan6, Status LEDs and so on.

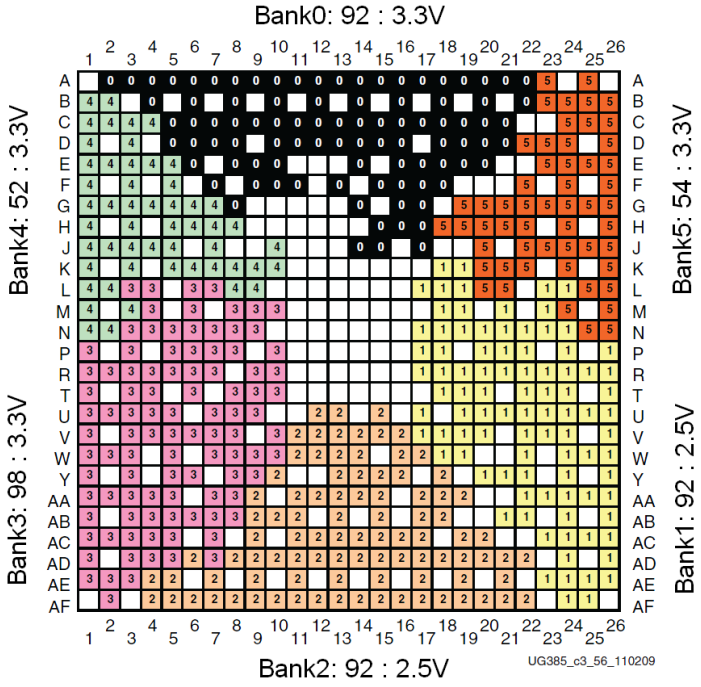

Figure7 Bank diagram for XC6SLX100-FGG676

The other 4 banks with 296 IOs in all (148 LVDS pairs) are used for the connections to Mimosa sensors in LVDS33 I/O standard, there are 6 detector layers for every Spartan6 FPGA which gives a request of 6*25=150 LVDS pairs, the shortage of two LVDS signals will be solved by employing another two LVDS25(compatible with LVDS33) pairs from bank2 which are assigned to the RSTB inputs of Mimosa sensors.

Configuration

There are two approaches for the FPGA configuration which is illustrated in Figure8: via JTAG interface during the development and commissioning phase (debug mode), or letting

Virtex6 FPGA configure the two Spartan6 FPGAs with the data written into the onboard flash or System ACE CF card (normal mode). For configuration with JTAG, one could select the onboard JTAG interface (JP1) or JTAG chain from Virtex6 DEV board, the two Spartan6 are serialized into the same JTAG chain with jumpers to bypass separately; for the slave serial configuration of Spartan6 by Virtex6, besides the configuration clock and data input, there are three other signals (PROGRAM_B/DONE/INIT_B) for the control and monitoring of configuration progress.

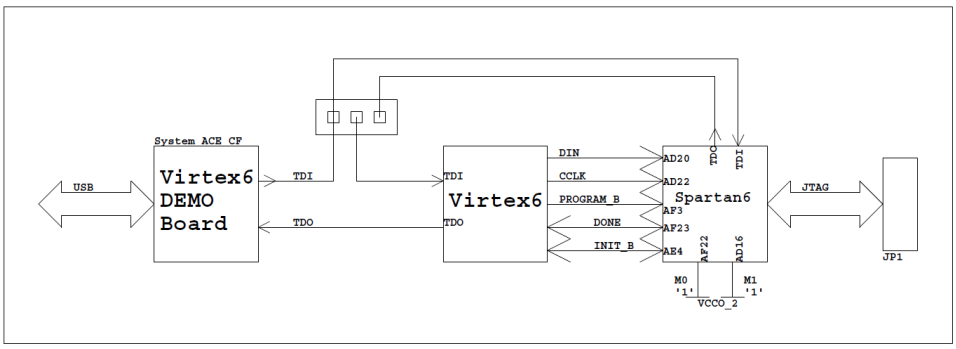

Figure8 Configuration of Virtex6/Spartan6

Power supply

Three voltages are needed for FPGAs on Adapter board: 1.2V core voltage and 2.5V/3.3V I/O voltage, 3 corresponded DC/DC converters with 10A max output current are adopted, vertical mounting type for the DC/DC converters is selected to save PCB areas. To be compatible with Virtex6 DEV board, the same MOLEX power connector is used for the 5V input of these converters which is from a 5V/10A AC/DC module.

The Auxiliary supply voltage (V_{CCAUX}) of Spartan6 is configurable with a jumper between 2.5V and 3.3V, the former value allows the compatibility of 2.5V input signals for a 3.3V I/O bank, the latter one gives the possibility of using JTAG chain from Virtex6 board because the JTAG module is powered by V_{CCAUX}.

For the 2.5V/3.3V power supply, it's also possible for them to be provided by the Virtex6 DEV board, depending on the power consumption and current limitations.

Clock resources

Spartan6 FPGAs will be responsible for the 160MHz clock inputs of Mimosa sensors and the reference clocks of optical transceivers, or probably some reference clocks to Virtex6 for data transmission depending on the communication protocol. There are two onboard oscillators common for both Spartan6 FPGAs, which can be optionally used directly or as the internal PLL/DCM inputs to generate different frequencies for different modules, also there are connections from Virtex6 board to the global clock inputs of Spartan6 allowing for deriving clock sources from Virtex6 for synchronization operations.

Spare I/Os

There are 184 I/Os from Bank1 and Bank2, except for those occupied by the connections to FMC connector of Virtex6 DEV board, the extra tens of I/Os are used as:

1. 8 LVDS pairs interconnected between two Spartan6 FPGAs.
2. 14 LVDS pairs connected to Termination board for RSTB, Optical Transceiver or as backup.
3. 2/3 used for status LED indication for debug.
4. Signals connected to 20-pin header J8, maybe used as trigger inputs or other purpose.

PCB specifications

The PCB board with a total thickness of 1.61mm has 8 layers: 5 signal layers, 2 power layers and 1 ground layer, Figure9 gives the layer stackup diagram. Figure10 shows the setup for 100ohm characteristic impedance of differential trace for every signal layer.

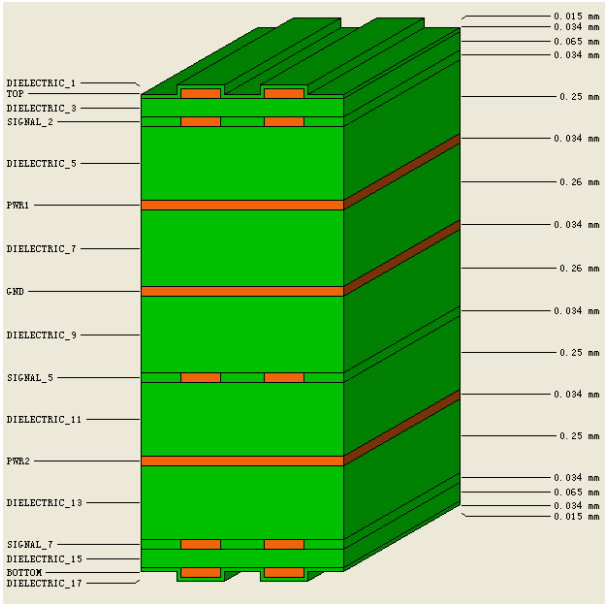

Figure9 PCB Layer stackup

Basic | Dielectric | Metal | Z0 Planning | Custom View

	Layer Name	Usage	Thickness th	Er	Diff Z0 ohm	Width th	Gap th
1	DIELECTRIC_1	Solder Mask	0.6	1			
2	TOP	Signal	1.35	<Auto>	100	10	5.105
3	DIELECTRIC_3	Substrate	2.559	4.5			
4	SIGNAL_2	Signal	1.35	<Auto>	100	5	6.142
5	DIELECTRIC_5	Substrate	9.843	4.5			
6	PWR1	Solid Plane	1.35	<Auto>			
7	DIELECTRIC_7	Substrate	10.236	4.5			
8	GND	Solid Plane	1.35	<Auto>			
9	DIELECTRIC_9	Substrate	10.236	4.5			
10	SIGNAL_5	Signal	1.35	<Auto>	100	5	9.526
11	DIELECTRIC_1	Substrate	9.843	4.5			
12	PWR2	Solid Plane	1.35	<Auto>			
13	DIELECTRIC_1	Substrate	9.843	4.5			
14	SIGNAL_7	Signal	1.35	<Auto>	100	5	6.142
15	DIELECTRIC_1	Substrate	2.559	4.5			
16	BOTTOM	Signal	1.35	<Auto>	100	10	5.105
17	DIELECTRIC_1	Solder Mask	0.6	1			

Figure10 Characteristic impedance of differential trace

The minimum trace width and clearance of the PCB is set to 5mils, the smallest via has a hole diameter of 12mils and pad size of 24mils.

1.4 Termination board

Two termination boards are needed for every Adapter board. The Termination board is mainly used for the signal fan out from the 500-pin high density FMC connector to 6 stacked RJ45 modular jacks, also for the concern of high data flow rate another optical transceiver utilizing the Virtex6 MGT signals is included, the system diagram is shown in Figure11.

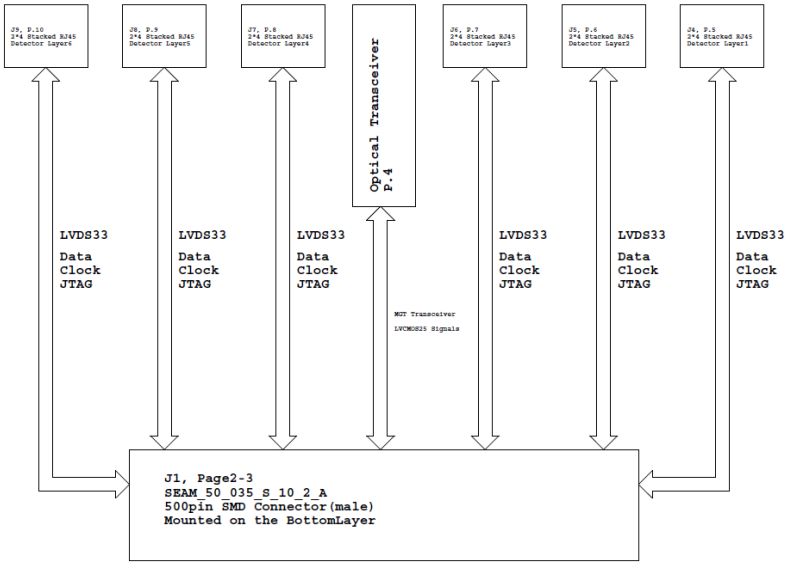

Figure11 Diagram of Termination board

For every detector layer, there are 6 LVDS output signals:

- TDI | TCK | TMS, for JTAG chain,
- CKR, readout clock for Mimosa
- START, synchronization instruction signal
- RSTB, Asynchronous reset;

Because not all LVDS signals can be configured as LVDS output, so these 6 signals should be taken care when signal reallocation needed.

There are 4 spare signals for every detector layer which can be used as digital control signals for future functions, depending on the firmware configuration, these 4 I/Os could be LVCMOS2.5 I/Os or LVDS25 inputs.

Note: the 4 spare I/O for layer3 are occupied by the control signals of optical transceiver.

Grounding

The signal ground of every detector layer is connected to the digital ground of readout electronics through a 0 ohm resistor or a ferrite bead, which allows different configurations of grounding schemes like single port or multi ports grounding, it also helps to solve ground loop problem.

The metal shell of every modular RJ45 Jack which will contact the shielding layer of twist pair cables could also be easily configured with a jumper for the grounding connection.

PCB specifications

The PCB board with a total thickness of 1.51mm has 4 layers: 3 signal layers and 1 power/ground plane layer, Figure12 gives the layer stackup diagram. Figure13 shows the setup for 100ohm characteristic impedance of differential trace for every signal layer.

To be easily fit into the 19’ crate, the width of Adapter board is set to 16’ with a symmetric distribution of mounting holes, RJ45 jacks and so on, which makes it possible to fix the boards of top and bottom side together.

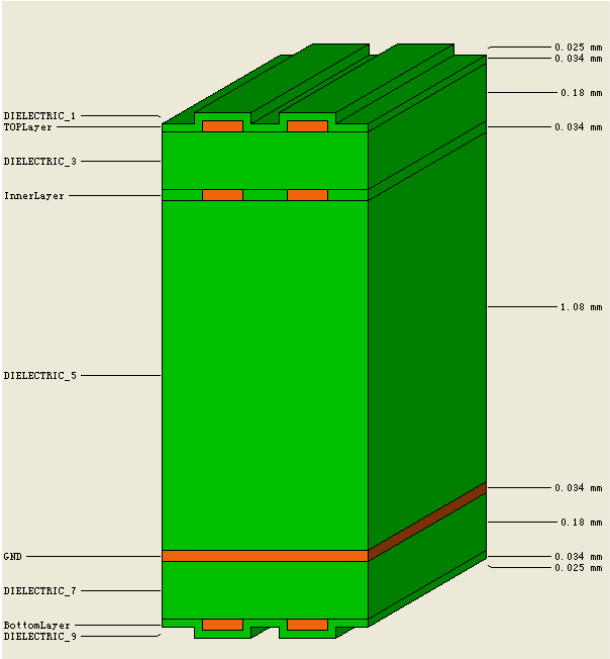

Figure12 PCB Layer stackup

Basic | Dielectric | Metal | Z0 Planning | Custom View

	Layer Name	Usage	Thickness th	Er	Diff Z0 ohm	Width th	Gap th
1	DIELECTRIC_1	Solder Mask	1	1			
2	TOPLayer	Signal	1.35	<Auto>	100	13	5.029
3	DIELECTRIC_3	Substrate	7.087	4.5			
4	InnerLayer	Signal	1.35	<Auto>	100	5	5.993
5	DIELECTRIC_5	Substrate	42.52	4.5			
6	GND	Solid Plane	1.35	<Auto>			
7	DIELECTRIC_7	Substrate	7.087	4.5			
8	BottomLayer	Signal	1.35	<Auto>	100	7	5.008
9	DIELECTRIC_9	Solder Mask	1	1			

Figure13 Characteristic impedance of differential trace

The minimum trace width and clearance of the PCB is set to 5mils, the smallest via has a hole diameter of 12mils and pad size of 24mils.

1.5 Bill of material

Table1 Bill of Material

DEVICE	PACKAGE	VALUE	QTY	Varenummer
Ceramic Capacitor	SM/C0402	0.47uF,1.5nH<ESL,10mΩ<ESR<60mΩ	300	
Ceramic Capacitor	SM/C0603	0.1uF	100	

Ceramic Capacitor	SM/C0805	4.7uF,2nH<ESL,10mΩ<ESR<60mΩ	200	
Tantalum Capacitor	7343/D	470uF,5nH<ESL,10mΩ<ESR<60mΩ	60	
Resistor	SM/R0603	0	40	
Resistor	SM/R0603	100	30	
Resistor	SM/R0603	33	30	
Resistor	SM/R0603	330	20	
Resistor	SM/R0603	4.7K	60	
Resistor	SM/R0603	4.75K	40	
LED	0805	Red/Green/Yellow	20	
Crystals	5mmx7mm	32MHz	3	
Ferrite Bead	SM0603	3A	20	
XCS6SLX100	FGG676	speed level >= 2	6	
DPDT_SW	1201_RA	1201M2S3CQE2	3	1437699
DC/DC	Vertical	LSN-3.3/10-D5-C	3	1423462
DC/DC	Vertical	LSN-2.5/10-D5-C	3	__
DC/DC	Vertical	LSN-1.2/10-D5-C	3	__
JTAG Connector		Molex_87831-1420	3	7472285
SEAM-40-03.5-S-10-2-A		CONNECTOR, MALE, 400WAY	6	1667983
SEAM-50-03.5-S-10-2-A		CONNECTOR, MALE, 500WAY	6	1667987
SEAF-50-05.0-S-10-2-A		CONNECTOR, FEMALE, 500WAY	6	1667966
molex_39301060		DUAL ROW, 6WAY, Power Connector	3	1697135
MOLEX39-01-2060		RECEPTACLE, MINI-FIT, 6WAY, CRIMP	3	151868
TYCO 5569262-1		2*4 stacked RJ45	36	1162485
tyco6367035-1		SFP Cage shell1 (optional)	6	1629986
tyco6367034-1		SFP Cage shell2 (optional)	6	1629985
SFP-1367073-1		SFP Cage 20PIN Connector(optional)	6	1629987

1.6 Mechanical Integration

19’ Crate,
5V Power supply
12V power supply
USB interface/adapter/cable (JTAG, UART, USB)
Ethernet adapter/cable
Virtex6 DEV board
Adapter board
Termination board

2. Firmware

For the two Spartan6 FPGAs, firmware should be totally identical except that they have different pin-map files.

2.1 JTAG interface

2.2 Trigger

2.3 Data sparsification

2.4 Optical transceiver

2.5 Petalinux application

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3. Software

3.1 JTAG control

3.2 Data recovery

3.3 Display

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4. Commissioning

4.1 ITB test board

4.1 Parallel readout

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References

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2. http://www.xilinx.com/products/devkits/EK-V6-ML605-G.htm
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