PHASE-1
User Manual

PRELIMINARY VERSION

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PHASE-1

Document history		
Version	Date	Description
1.0	July 2008	Creation, based on Mimosa22 version

PHASE-1 chip			
Version	Date	Description	Comments
1.0	Submitted July 2008	AMS C35B4/Opto 640x640pixels, pitch 30µm, readout 160 MHz	Preliminary version

PHASE-1

1 Introduction

PHASE-1 is the intermediate version of the monolithic integrated detector to be used in the STAR experiment at RICH. The architecture is based on Mimosa22 with faster readout and larger matrix of pixels. The design process is Austria Mikrosysteme AMS-C35B4/OPTO which uses 4 metal- and 2 poly- layers. The thickness of the epitaxial layer is 14 µm. The design tools are provided by CMP (Cadence DFII, v5.1, IUS v 5.7, SoC v4.1 LDV v5) as well as the verification tools (Diva, Assura v3.17, Calibre v2007.02). The chip was submitted as Engineering Run on July 2008.

The size of the chip is 19,52 mm x 20,93 mm, but the active area is 19.2mm x 19.2 mm and contains an array of 640 x 640 pixels with a pitch of 30 µm. An abstract view of the die is depicted in Figure 1 for the sake of clarity the picture is not in scale and does not reflect the real layout even if it shows all the main blocks and the chip architecture.

Details how to program the internal functionalities of the chip are in Section 2, the information to operate the chip are in the Section 3 and the layout of the padring with chip bonding are in the Section 4.

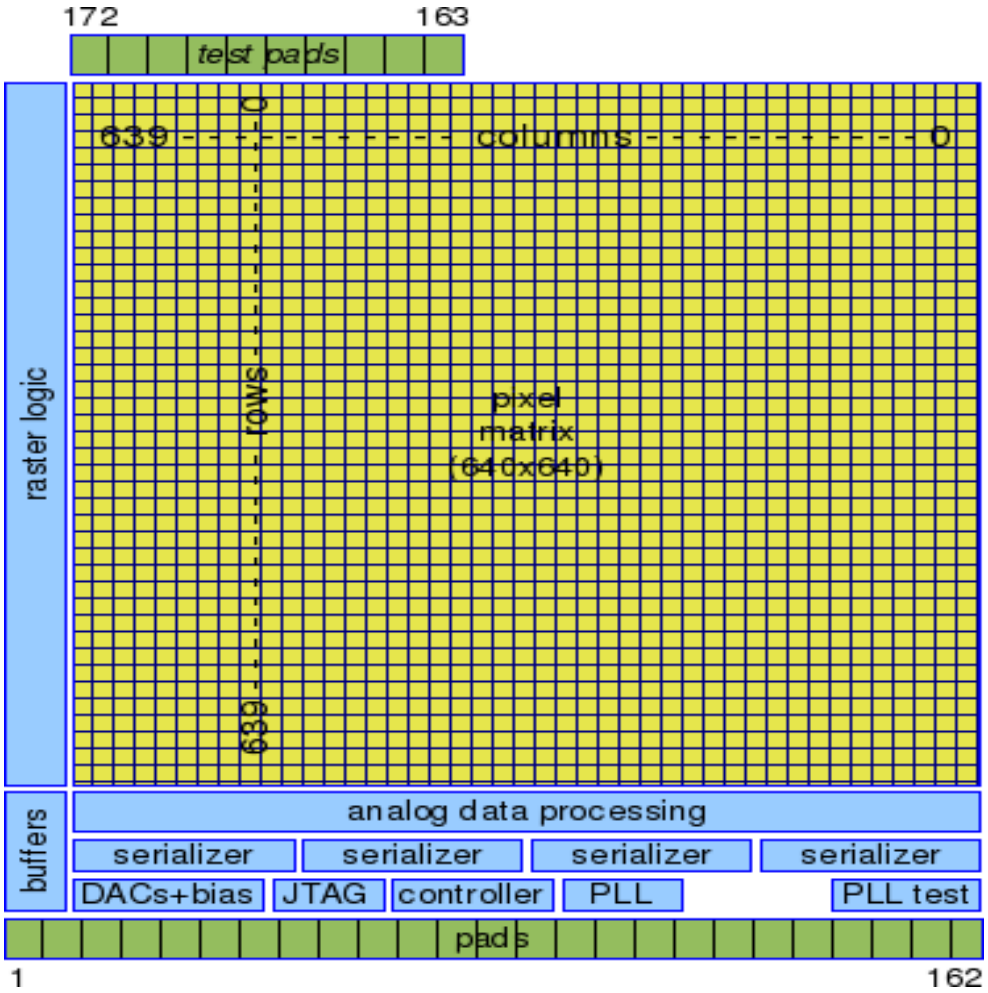


Figure 1 -- abstract view of the die, it does not reflect the real floorplan since the scale factor is altered for sake of clarity but it shows all the main blocks and the chip architecture

2 Control Interface

The control interface of PHASE-1 complies with Boundary Scan, JTAG, IEEE 1149.1 Rev1999 standard. It allows the access to the programmable internal registers. On power on, an internal reset Power-On –Reset is automatically generated for the control interface, the initial status of the Test Access Port (TAP) is Test-Logic-Reset and the ID register is selected.

PHASE-1 has been designed in order to be fully tuneable via the control interface, nevertheless some voltages level might be forced from the external pads.

2.1 JTAG Instruction Set

The Instruction Register of the JTAG controller is loaded with the code of the desired operation to perform or with the code of the desired data register to access.

Instruction	5 Bit Code$_{16}$	Selected Register	Notes
EXTEST	01	BSR	JTAG mandatory instruction
HIGHZ	02	BYPASS	JTAG mandatory instruction
INTEST	03	BSR	JTAG mandatory instruction
CLAMP	04	BYPASS	JTAG mandatory instruction
SAMPLE_PRELOAD	05	BSR	JTAG mandatory instruction
ID_CODE	0E	DEV_ID register	User instruction
BIAS_GEN	0F	BIAS_DAC	User instruction
PATTERNL0_REG	10	LINEPATL0_REG	User instruction
DIS_LATCH	11	DIS_DISCRI	User instruction
SEQ_REG	12	SEQUENCER_REG	User instruction
CTRL_REG	13	CONTROLER_REG	User instruction
PATTERNL1_REG	14	LINEPATL1_REG	User instruction
NU1	15	(1)	Reserved, Not Used
NU2	16	(1)	Reserved, Not Used
NU3	17	(1)	Reserved, Not Used
NU4	18	(1)	Reserved, Not Used
NU5	19	(1)	Reserved, Not Used
NU6	1A	(1)	Reserved, Not Used
NU7	1B	(1)	Reserved, Not Used
NU8	1C	(1)	Reserved, Not Used
RO_MODE1	1D	ReadOut Mode 1	User instruction
RO_MODE0	1E	ReadOut Mode 0	User instruction
BYPASS	1F	BYPASS	JTAG mandatory instruction

(1) Instruction codes implemented but not the corresponding registers. To be fixed in the next version.

2.2 JTAG Register Set

JTAG registers are implemented with a Capture/Shift register and an Update register. JTAG standard imposes that the last significant bit of a register is downloaded/shifted first.

Register Name	Size	Access	Notes
INSTRUCTION REG	5	R/W	Instruction Register
DEV_ID	32	R Only	
BYPASS	1	R Only	

BSR	10	R/W	
BIAS_DAC	120	R/W	Previous value shifted out during write
RO_MODE0	8	R/W	Previous value shifted out during write
RO_MODE1	8	R/W	Previous value shifted out during write
CONTROL_REG	40	R/W	Previous value shifted out during write
SEQUENCER_REG	128	R/W	Previous value shifted out during write
DIS_DISCRI	640	R/W	Previous value shifted out during write
LINEPATL0_REG	640	R/W	Previous value shifted out during write
LINEPATL1_REG	640	R/W	Previous value shifted out during write
NU1,NU2,…,NU8	0	-	Not implemented. For future use

2.2.1 Instruction Register

The Instruction register is a part of the Test Access Port Controller defined by the IEEE 1149.1 standard. The Instruction register of PHASE-1 is 5 bits long. On reset, it is set with the ID_CODE instruction. When it is read the 2 last significant bits are set with the markers specified by the standard, the remaining bits contain the current instruction.

X	**X**	**X**	**1**	**0**

2.2.2 DEV_ID Register

The Device Identification register is a read-only 32-bit register. When selected by the ID_CODE instruction or after the fixed value is shifted via TDO, the JTAG serial output of the chip.

PHASE-1 ID_CODE register value is *0x50483101*.

Bit #	**Bit Name**	**Purpose**	**Default value Code$_{16}$**		
31-0	ID_CODE	Device Identification register	50483101	*ASCII*	*HEX*
				‘P’	50
				‘H’	48
				‘1’	31
				<SOH>	01

2.2.3 Bypass Register

The Bypass register consists of a single bit scan register. It is selected when its code is loaded in the Instruction register, during some actions on the BSR and when the Instruction register contains an undefined instruction.

2.2.4 Boundary Scan Register

The Boundary Scan Register, according with the Jtag instructions, tests and set the IO pads. The PHASE-1 BSR is 10 bits long and allows the test of the following input and outputs pads.

Bit #	**Corresponding Pad**	**Type**	**Signal**	**Notes**
8	CkPLL	Input	CkPLL	PLL Clock
7	CkCMOS	Input	CkCMOS	CMOS Clock
6	LVDS CkRdLn/CkRdLp	Input	ClkLvds	Resulting CMOS signal after LVDS Receiver

5	START	Input	START	Readout : Input synchronisation
4	SPEAK	Input	SPEAK	Active Readout Marker & Clock
3	MK_CLK_A	Ouput	MK_CLK_A	Readout : Analogue Marker & Clock
2	CLKA	Ouput	CLKA	Readout Analogue Clock
1	Tst2Pad	Ouput	Tst2Pad	Readout Test Pad 2
0	Tst1Pad	Ouput	Tst1Pad	Readout Test Pad 1

2.2.5 BIAS_DAC Register

The BIAS_DAC register is 128 bit wide; it sets simultaneously the 16 DAC registers.

As show bellow these 8-bit DACs set voltage and current bias. After reset the register is set to 0, a value which fixes the minimum power consumption of the circuit. The current values of the DACs are read while the new values are downloaded during the access to the register. An image of the value of each DAC can be measured on its corresponding test pad.

Bit range	DAC #	DAC Internal Name	DAC purpose	Corresponding Test Pad
127-120	DAC15	IKIMO	External circuit monitoring	VKIMO
119-112	DAC14	IPIX	Pixel source follower bias	IPIX
111-104	DAC13	IVTST2	Test Level, emulates a pixel output	VTEST2
103-96	DAC12	IVTST1	IDEM	VTEST1
95-88	DAC11	IDIS2	Discriminator bias 2	IDIS2
87-80	DAC10	IDIS1	Discriminator bias 1	IDIS1
79-72	DAC9	IVDREF2	Discriminator Reference 2	VDREF2
71-64	DAC8	IVDREF1	Discriminator Reference 1	VDREF1
63-56	DAC7	IAnaBUF	Analogue Buffer bias	IAnaBUF
55-48	DAC6	ILVDS	LVDS PAD bias	ILVDS
47-40	DAC5	ILVDSTX	LVDS PAD bias	ILVDSTX
39-32	DAC4	ID2PWRS	Discriminator bias 2 (mode low consp.)	
31-24	DAC3	ID1PWRS	Discriminator bias 1 (mode low consp.)	
23-16	DAC2	IBufBias	Ref&Tst Buffer bias	BUFBIAS
15-8	DAC1	IPwrSWBias	Discriminator Power Pulse bias	PWRSWBIAS
7-0	DAC0	ICLPDISC	Discriminator Clamping bias	DISCLP

2.2.6 RO_MODE0 Register

The RO_MODE0 registers are 8 bits large; they allow the user to select specific digital mode of the chip.

Bit #	Bit Name	Purpose	Basic configuration value	
7	En_TstBuf	Enable the internal injection of VTEST	0	External injection of VTEST
6	En_HalfMatrx	Set the row shift register to 320 in place of 640 bits.	0	Normal mode, 640 row shift register selected
5	DisLVDS	Disable LVDS and active clock CMOS.	0	LVDS selected
4	En_LineMarker	Add two rows at the end of matrix for a chip Readout: The LINEPAT_REG register is selected to emulate discriminators outputs. For analogue outputs, the 2 Test Levels, VTEST1 and VTEST2 are selected which emulate a pixel output.	0	Normal mode
3	MODE_SPEAK	Select Marker signal or Readout Clock for digital and analogue data (MK_CLKA and MK_CLKD pads)	0	Marker signal active
2	Pattern_Only	Test Mode: Select LINEPAT_REG to emulate discriminators outputs	0	Normal mode
1	En_ExtStart	Enable external START input synchronisation	0	Normal mode

		(1)		
0	JTAG_Start	Enable Jtag START input synchronisation (2)	0	

(1) The minimum wide of asynchronous external START is 2000 ns, and this signal is active at high level.

(2) When En_ExtStart is disabled, it's possible to generate internal START by accessing JTAG_Start bit. JTAG_Start signal is realized by three JTAG access: First step, this bit is set to 0, second step it is set to 1, and at last it is set to 0.

2.2.7 RO_MODE1 Register

The RO_MODE1 registers are 8 bits large; they allow selecting specific analogue mode of the chip.

Bit #	Bit Name	Purpose	Basic configuration value	
7	En_Pll	Enable internal pll	0	
6	En_AnaCol	Enable analog output	0	
5	En_PixScan	Enable scan pixel mode	0	
4	DisBufRef	Disable the internal reference	0	Select Internal Buffer
3	En_HS	Enable High speed mode	0	Select low speed mode
2	En_AOP_Disc	Enable the Power pulse Amplifier	0	Normal mode
1	En_Pulse_Discri	Enable the discri power pulse mode	0	Normal mode
0	En_TstDis	Enable the discri. test mode	0	Normal mode

2.2.8 CONTROL_REG Register

The CONTROL_REG registers are 40 bits large; they allow setting parameters of the readout controller.

Bit #	Bit Name	Purpose	Basic configuration value $Code_{16}$	
39-36	NU	Reserved, Not Used	0	
35-33	SelPad2	Selection bit of Test2Pad	0	MK_Test_D signal
32-30	SelPad1	Selection bit of Test1Pad	0	MK_Test_A signal
29-20	RowMkLast	Row number of the frame. It depends of readout mode. When the En_HalfMatrx mode is active, the value is 0x013F otherwise 0x027F. When the En_LineMarker mode is active, add two rows at the end of matrix.	027F	Normal mode, the number of row matrix is 640.
19-10	RowMkd	Selection parameter of row for digital marker (MK_Test_D)	0	Digital marker place is first row of matrix during the readout
9-0	RowMka	Selection parameter of row for analogue marker (MK_Test_A)	0	analogue marker place is first row of matrix during the readout

The purpose of this array is to describe the internal signals which can be checked using 2 test pads (Tst1Pad and tst2Pad). The internal signals can be selected with SelPad1 and SelPad2 bits.

SelPad1	Tst1Pad	Purpose	SelPad2	Tst2Pad	Purpose
0	MK_Test_A	Analogue marker is delayed of 500 ns respect to MK_A signal. This signal rises up at the beginning read phase and falls down at the end of Calib phase. It depends of RowMka selection	0	MK_Test_D	Digital marker corresponding to last serialized digital data. It depends of RowMkd selection parameter.

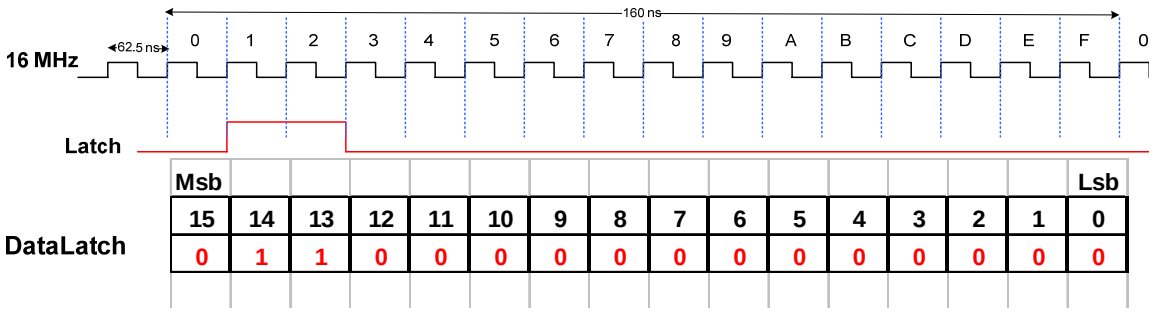
		parameter.			
1	Mk_Rd	Analogue marker corresponding to Rd phase of readout pixel. It depends of RowMka selection parameter	1	PwrOns	Same signal as PwOn, but shifted of 16 main clock
2	Mk_Calib	Analogue marker corresponding to Calib phase of readout pixel. It depends of RowMka selection parameter	2	PwOn	Activate power supply for pixel
3	Ckdiv10	Main Clock is devised by 10	3	SlcRowInt	Connect pixel output to common column
4	MK_A	Analogue marker corresponding to readout pixel sequence. It depends of RowMka selection parameter.	4	Clp	Set reference voltage for clamping
5	Clp	Set reference voltage for clamping	5	RstDiode	Set reference voltage for diode
6	Latch	Latch state of the discriminator	6	Rd	Sample before clamping
7	CkDiv16	Ckdiv10 is devised by 16	7	Calib	Sample after clamping

2.2.9 SEQUENCER_REG Register

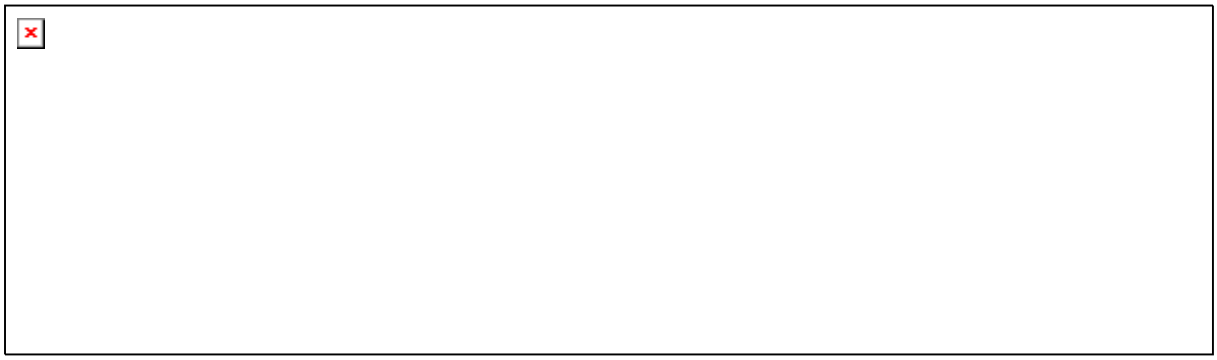
The SEQUENCER_REG registers are 128 bits large; this register contains all parameters to generate readout pixel and discriminator sequence.

Bit #	Bit Name	Purpose	Basic configuration value $Code_{16}$	Signal Name
127-112	DataRdPix	Connect pixel output to common column	7FFF	Slct_Row_Int
111-96	DataRst1	Set reference voltage for diode	0040	Rst
95-80	DataClp	Set reference voltage for clamping	01C0	Clamp
79-64	DataCalib	Sample after clamping	3C00	Calib
63-48	DataRdDsc	Sample before clamping	001C	Read
47-32	DataLatch	Latch state of the discriminator	6000 (1)	Latch
31-0	DataPwrOn	Activate power supply for pixel	7FFFFFFF	Pwr_On

(1) Example: Generation of Latch Signal

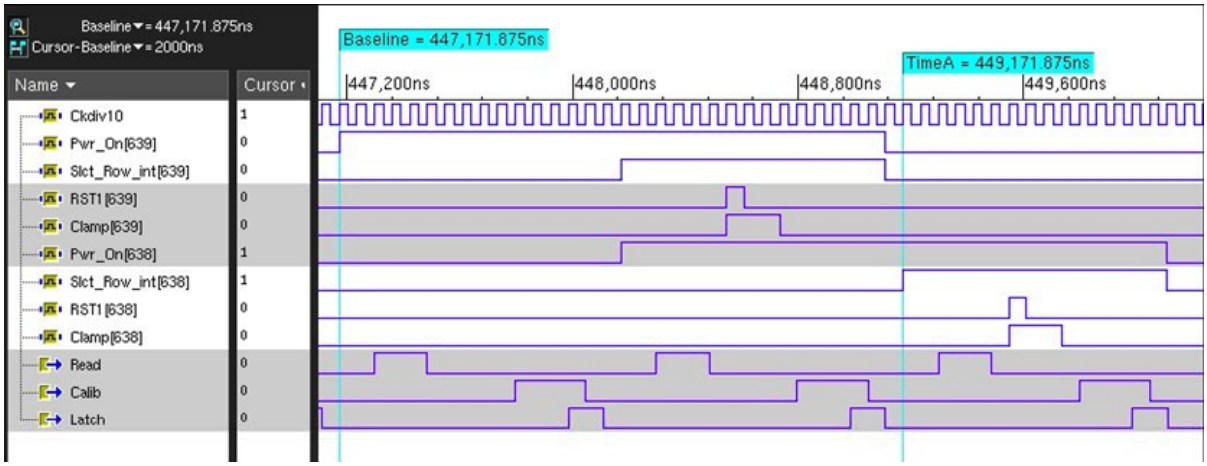


- Related timing with $f_{Ckdiv10}$=16 MHz (Read, Calib, Latch signals are used by the column readout circuitry).



The Rst signal is not used for pixel.

- This is readout sequence of the pixel and discriminator for 2 successive rows of matrix. In the wave form, the indexation of internal signal vectors is reversed compared with the Phase1 functional view (for example, the signal Pwr_On[639] corresponds to the row at the top of matrix).



2.2.10 DIS_DISCRI Register

The DIS_DISCRI register is 640 bits large. The purpose of this register is to disable the discriminator on a specific column if it is noisy, by gating Latch signal and setting the output discriminator at 0.

The default value of the DIS_DISCRI register is 0; it means that all discriminators are activated. Setting a bit to 1 disables the corresponding discriminator. In Phase1, the DisableLatch<639> is on the left hand side while DisableLatch<0> is on the right hand side.

639 (Msb)	0 (Lsb)
DisableLatch<639>	DisableLatch<0>

2.2.11 LINEPAT0_REG Register

The LINEPAT0_REG register is 640 bits large but only the first 630 are programmable. The purpose of this register is to emulate discriminators outputs rows in *En_LineMarker* and Pattern_Only modes.

When *Pattern_Only* is active, the values stored in the pixel matrix are ignored and the value of LINEPAT0_REG is sent to the output. This is a test mode which emulates the (digital) pixel response with the contents programmed into the LINEPAT0_REG register in order to verify the digital processing. The pattern is alternated with the contents of the LINEPAT1_REG.

In the *En_LineMarker* mode, it adds two rows at the end of matrix for a readout chip and the LINEPATL0_REG register is read to emulate the discriminators outputs of these two supplementary rows. This mode allows generating pattern marker in matrix data frame to detect chip readout desynchronization.

Bit #	Bit Name	Purpose	Basic configuration value $Code_{16}$
639-630	Not used	Reserved for the frame counter (read only)	200(1)
629-0	LinePatL0Reg	Emulate discriminators rows	2AAAAA_AAAAAAAA_AAAAAAAA_AAAAAAAA(2)

(1) This code is valid only after *START*

(2) Example of pattern used in simulation.

2.2.12 LINEPAT1_REG Register

The LINEPAT1_REG register is 640 bits large but only the first 630 are programmable. The purpose of this register is to emulate discriminators outputs rows in *En_LineMarker* and Pattern_Only modes.

When *Pattern_Only* is active, the values stored in the pixel matrix are ignored and the value of LINEPAT0_REG is sent to the output. This is a test mode which emulates the (digital) pixel response with the contents programmed into the LINEPAT0_REG register in order to verify the digital processing. The pattern is alternated with the contents of the LINEPAT1_REG.

In the *En_LineMarker* mode, it adds two rows at the end of matrix for a readout chip and the LINEPATL1_REG register is read to emulate the discriminators outputs of these two supplementary rows. This mode allows generating pattern marker in matrix data frame to detect chip readout desynchronization.

Bit #	Bit Name	Purpose	Basic configuration value $Code_{16}$
639-630	Not used	Reserved for the frame counter (read only)	200(1)
629-0	LinePatL1Reg	Emulate discriminators rows	155555_55555555_55555555_55555555(2)

(1) This code is valid only after *START*

(2) Example of pattern used in simulation.

3 Running Phase1

The following steps describe how to operate PHASE-1

3.1 After reset

On RstB active low signal:

- All BIAS registers are set to the default value, i.e. 0
- DIS_DISC is set to 0, i.e. all columns are selected
- RO_MODE0 is set to 0
- RO_MODE1 is set to 0
- CONTROL_REG is set to 0
- SEQUENCER_REG is set to 0
- LINEPATL0_REG is set to 0
- LINEPATL1_REG is set to 0
- JTAG state machine is in the Test-Logic-Reset state
- JTAG ID_CODE instruction is selected

Then the bias register has to be loaded.

The same for the RO_MODE0, RO_MODE1, CONTROL_REG, SEQUENCER_REG, LINEPATL0_REG, LINEPATL1_REG and DIS_DISC registers if the running conditions differ from defaults.

Finally the readout can be performed either in normal mode or in test mode.

3.2 Biasing Phase1

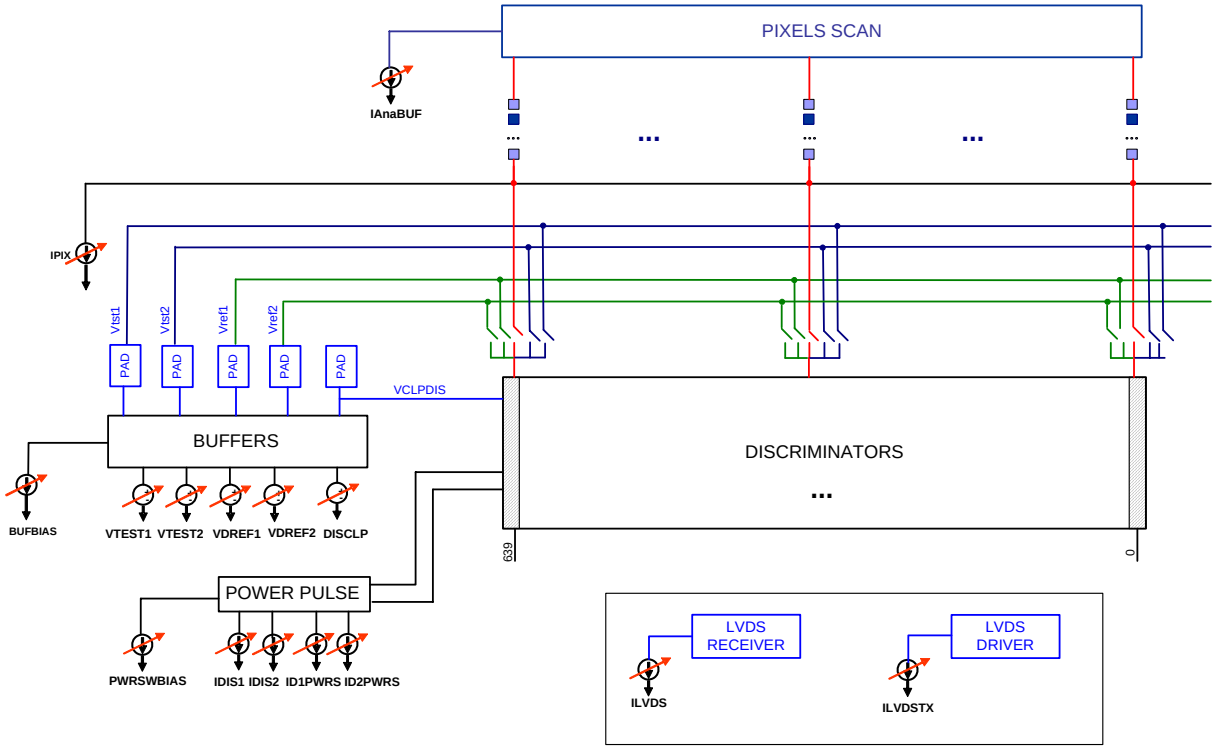
The BIAS_DAC register has to be loaded before operating Phase1.

The 16 DACs constituting this register are built with the same 8 bits DAC current generator which has a 1 µA resolution. Specific interfaces like current mirror for current sourcing or sinking and resistors for voltages, customise each bias output. The following table shows the downloaded codes which set the nominal bias.

Internal DAC Name	**Simulation**			**Resolution**	**Range**	**Experimental**
	$Code_{16}$ - $Code_{10}$	**DacInternal current-µA**	**Output value**			**$Code_{16}$ - $Code_{10}$**
IKIMO	64-100	100	1 V	10 mV	0 – 2.55 V	
IPIX	32-50	50	50 µA	1 µA	0 – 255 µA	
IVTST2	71-118	118	1.18 V	10 mV	1 – 1.5 V	
IVTST1	8C-118	118	1.18 V	250 µV	-32 – 32 mV	
IDIS2	20-32	32	5 µA	156 nA	0 – 255 µA	
IDIS1	20-32	32	10 µA	312 nA	0 – 255 µA	
IVDREF2	71-118	118	1.18 V	10 mV	1 – 1.5 V	
IVDREF1	80-118	118	1.18 V	250 µV	-32 – 32 mV(1)	
IAnaBUF	32-50	50	500 µA	10 µA	0 – 255 µA	
ILVDS	20-32	32	7 µA	218 nA	0 – 255 µA	
ILVDSTX	28-40	40	40 µA	1 µA	0 – 255 µA	
ID2PWRS	A-10	10	100 nA	10 nA	0 – 255 µA	
ID1PWRS	A-10	10	100 nA	10 nA	0 – 255 µA	
IBufBias	A-10	10	10 µA	1 µA	0 – 255 µA	
IPwrSWBias	A-10	10	10 µA	1 µA	0 – 255 µA	
ICLPDISC	64-100	100	2.1 V	10 mV	1.2 – 3.2 V	

(1) Referenced with respect to IVDREF2. The threshold voltage of the discriminators is ΔVth = Vref1-Vref2 and the relationship is Vref1=Vref2+ΔVth

Bias synthetic block diagram



3.3 Setting the Readout Configuration Registers

If the desired operating mode does not correspond to the default one, set RO_MODE0, RO_MODE1, CONTROL_REG, SEQUENCER_REG, LINEPAT0_REG, LINEPAT1_REG registers following the §2.2.6, §2.2.7, §2.2.8, §2.2.9 and §2.2.11.

3.4 Readout

3.4.1 Signal protocol

After JTAG registers have been loaded, the readout of PHASE-1 can be initialized with following signal protocol:

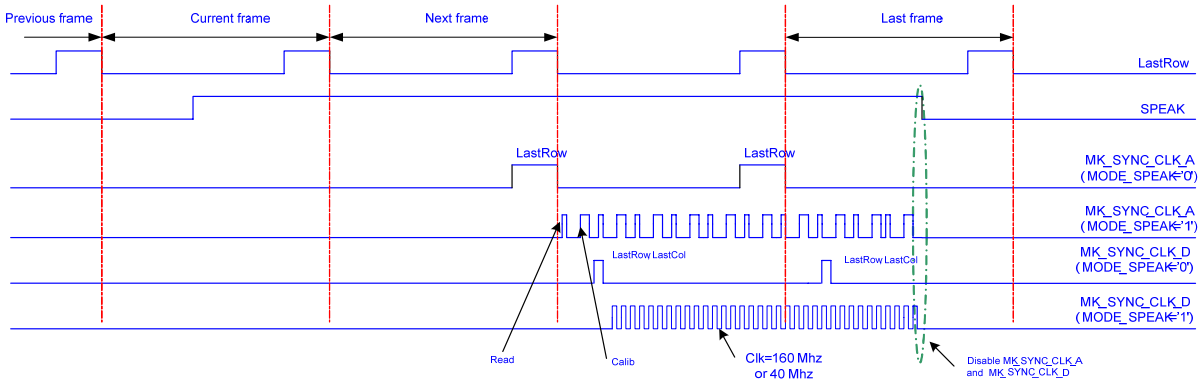
- Start readout clock (Master Clock 160 MHz);
- Initially set SPEAK signal to 0;
- Set to 1 the START signal for 2000 ns (minimum). During this step the internal reset is generated and then the clock dividers start to produce the *clkdiv10* (16 MHz) and *clkdiv* (1 MHz);
- The readout controller starts at the first falling edge of *clkdiv*.

Signal markers allow the readout monitoring and the data outputs (analogue and digital) sampling:

- CLKA and CLKD are running when readout controller starts. CLKA is a logic OR between Read and Calib signals and CLKD corresponds to 160 MHz (fast readout) or 40 MHz (slow readout);
- When SPEAK signal is active, markers of synchronisation for analogue and digital outputs are generated on MK_CLK_A and MK_CLK_D pads.

3.4.2 Successive frames and resynchronisation

Successive pixel frames are read meanwhile the readout clock is running.
The frame resynchronisation can be performed at any time by setting up the “START” token again.



SPEAK signal allows to generate markers signals which are used by DAQ. When SPEAK signal is set to 1 during the current frame an analogue marker appears on MK_SYNC_CLK_A pad and digital marker appears on MK_SYNC_CLK_D pad on next frame.

In the MODE_SPEAK=’0’ (see Figure 9, Figure 10), the MK_SYNC_CLK_A marker corresponds to last row of the frame and the MK_SYNC_CLK_D marker corresponds to last bit frame.

In the MODE_SPEAK=’1’, the MK_SYNC_CLK_A signal corresponds to a sampling clock for analogue outputs data (same as CLKA) which starts at the first row of frame. MK_SYNC_CLK_D signal corresponds to readout clock for digital data (same as CLKD) which starts at the first bit frame.

When SPEAK signal is set to 0, MK_SYNC_CLK_A and MK_SYNC_CLK_D are set to 0.

3.5 Analogue and digital Data Format

PHASE-1 uses the pads at the bottom edge for all its operations, whatever is collecting data from the pixels (using the pixels and the discriminators) or in test mode (reproducing at the outputs the pre-programmed patterns). All the digital signals to synchronize and programming the chip are necessary to operate successfully.

Analog outputs located on the top edge of the chip are not used for the normal operations. The main purpose is to characterize the pixels or to check the dead pixels. Therefore measurements on these pads deal with normal pixel signals as well as test signals (but they still require the synchronization and the markers) and it is activated on demand by setting to 1 the *En_AnaCol* bit in the RO_MODE1 register.

3.5.1 Normal mode data format

The digital part includes three blocks. One is JTAG controller interface which allows configure the internal registers used to readout chip. The second circuit generates the patterns necessary for addressing, resetting and double sampling of the signals in pixels in a column parallel way. The clock scans line by line at 1 MHz and latches the data in the output register which is divided in 4 parts each connected to one of the 4 main outputs.

Figure 11 shows the internal structure of the output register and the serializer. There are 2 levels of multiplexing, first one runs at full speed of 160 MHz and the second one (4:1) which is used mainly for test purpose runs at lower speed of 40 MHz. Because of these additional multiplexing, the output data are scrambled.

The Vref1 voltage is applied to the negative discriminator input during the read phase and the Vref2 voltage is applied during the Calib phase. The difference voltage Vref1 – Vref2 set the threshold of the discriminator. Voltages can be adjustable via 2 DACs or can be provided via 2 pads.

When *En_AnaCol* bit is set to ‘1’ in the RO_MODE1 register, the rightmost 8 columns of pixels are connected to the analog outputs via a voltage follower and the signal is available on the pads. To start the analog test, the *En_PixScan* must be set to ‘1’ in the RO_MODE1. The scanning of the matrix now starts and stripes of 8 pixels are connected to the analog output. The analog test is performed considering a reduced size of the array (about 640 rows x 8 columns), therefore it takes 80 frame acquisitions to analyze the full matrix. Figure 1 shows how to do the analog characterization and which parts of the matrix are under test for each frame.

The MK_CLKA is the synchronization marker for the analog outputs and it works like its digital homologue, see When *En_AnaCol* bit is set to ‘1’ it appears at the end of each frame, this signal is used to sample the analog

channel of the new frame on the next raising edge of CLKA. Further when the *En_PixScan* must be set to '1', this marker appears at the end of the frame for each submatrix.

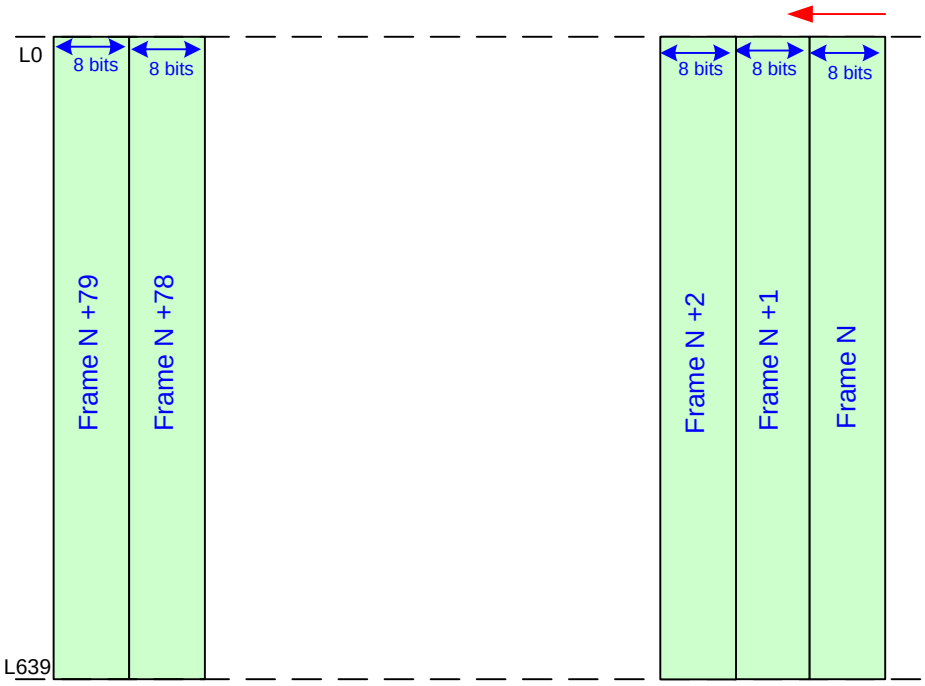


Figure 2 -- Analog characterization of the pixel: the matrix is divided in stripes of 8 columns and fully scanned at each frame, then swapped with the next block of 8 columns at right and so on until all the columns are analyzed.

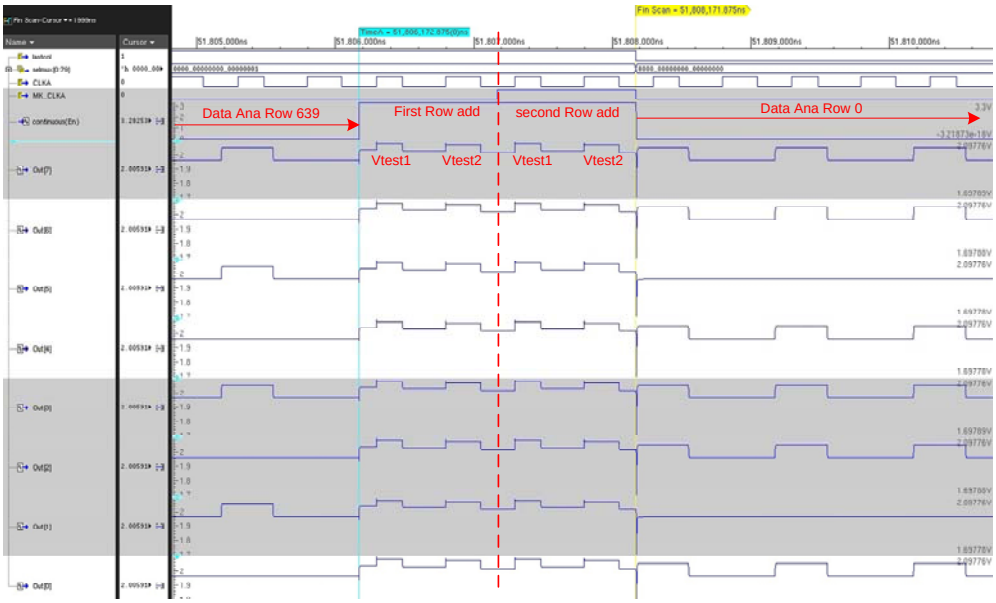


Figure 3 – Mode scan for analog output

3.5.2 Test mode data format

This test readout mode allows obtain the transfer function of discriminator and calibrate the pixel readout chain. During the test mode the pixel matrix is not connected to discriminators and output analogue buffers. Instead of this, two test levels Vtst1, Vtst2 are connected to discriminator inputs to emulate pixel signal.

The Vtst1 voltage is applied to the positive discriminator input during the Read phase and the Vtst2 voltage is applied during the Calib phase. Voltages can be adjustable via 2 DACs or can be provided via 2 pads. The difference voltage Vtst1 – Vtst2 corresponds to the pixel output signal.

3.6 PHASE-1 Timing Diagrams

PHASE-1 needs an initialization step before starting the normal acquisition. After the master reset, the JTAG should be loaded with configuration and bias settings, then the START signal begins the automatic scanning ad readout of the pixel matrix.

3.6.1 Normal Readout

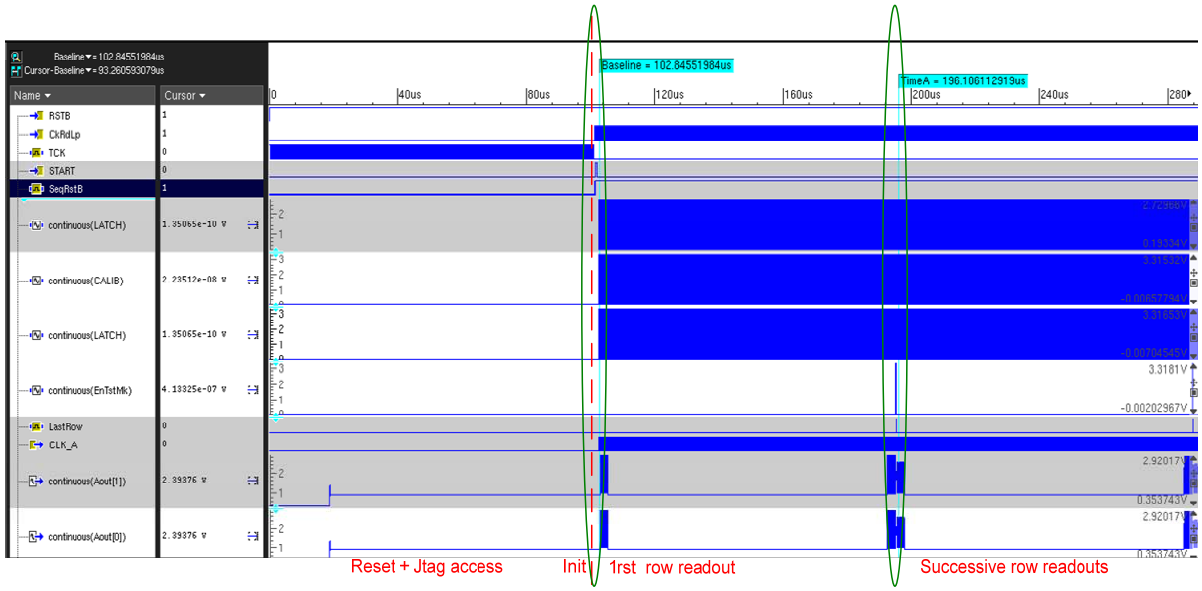


Figure 4 – Beginning of readout mode. after Reset and JTAG settings the data are immediately available at the main outputs. Subsequent frames are automatically handled by the internal logic

3.6.2 Readout synchronisation

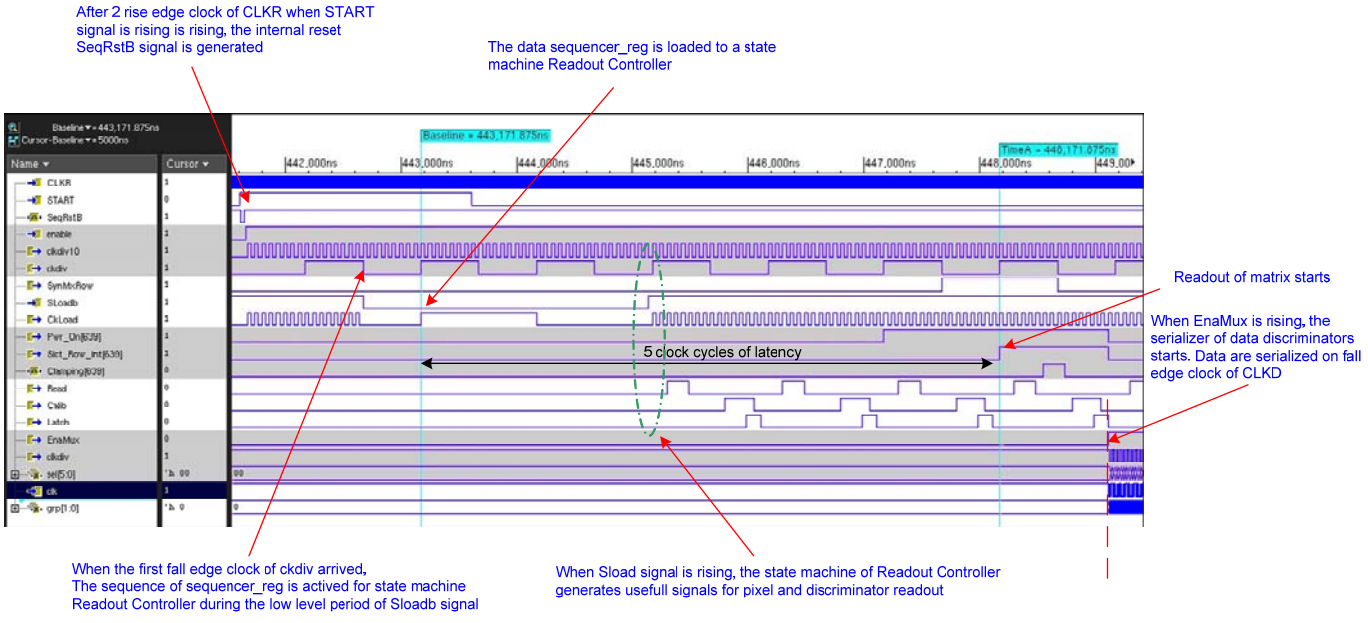


Figure 5 – zoom on readout start, after a latency of 5 *clkdiv* cycles, readout of matrix starts, the zone on the right will be expanded for clarity

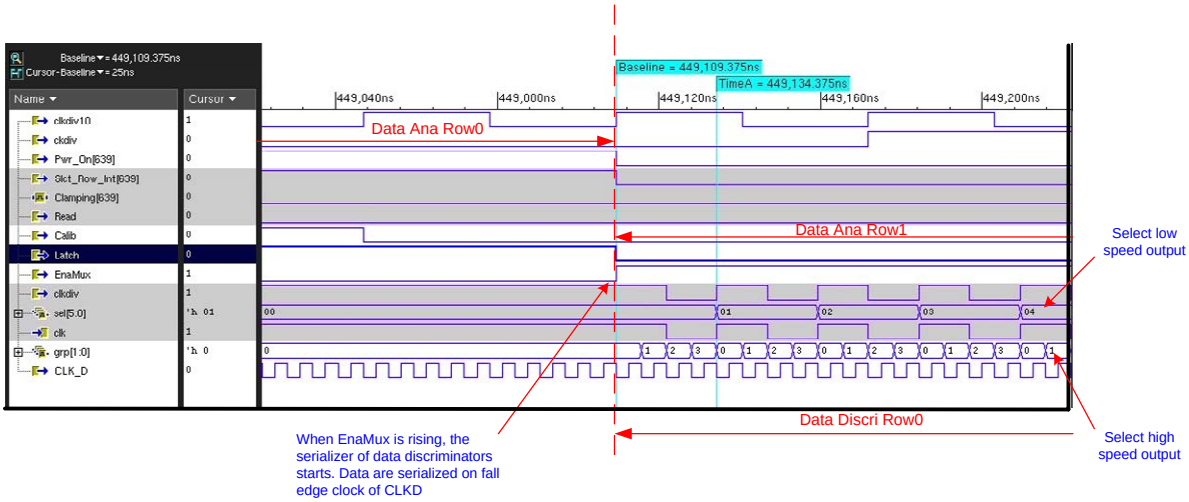


Figure 6 – start of the serializer, the latch signal enables the outputs. Data are sent on falling edge of CLKD. It is visible the readout of the first row and the beginning of the serialization.

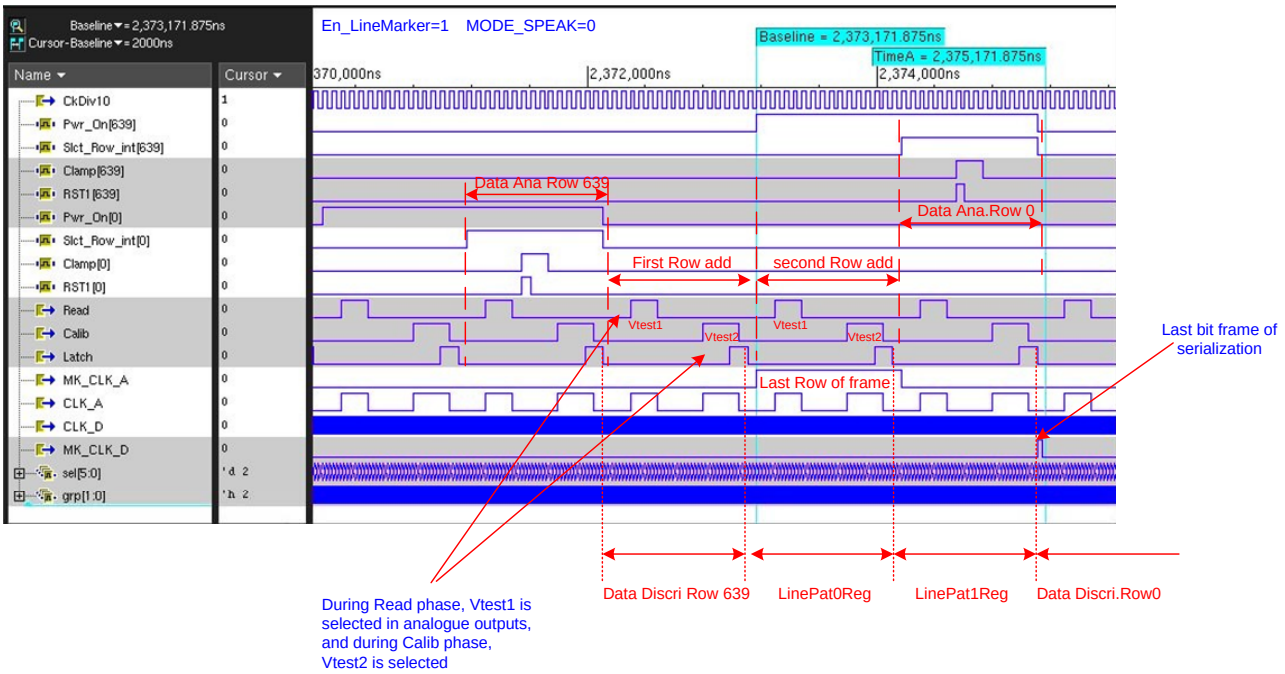


Figure 7 – interframe timing diagram shows the ending of frame and first row digital data serialization, when *En_LineMarker* is set to 1 and *MODE_SPEAK* is set to 0. These options are set via the *RO_MODE0* register.

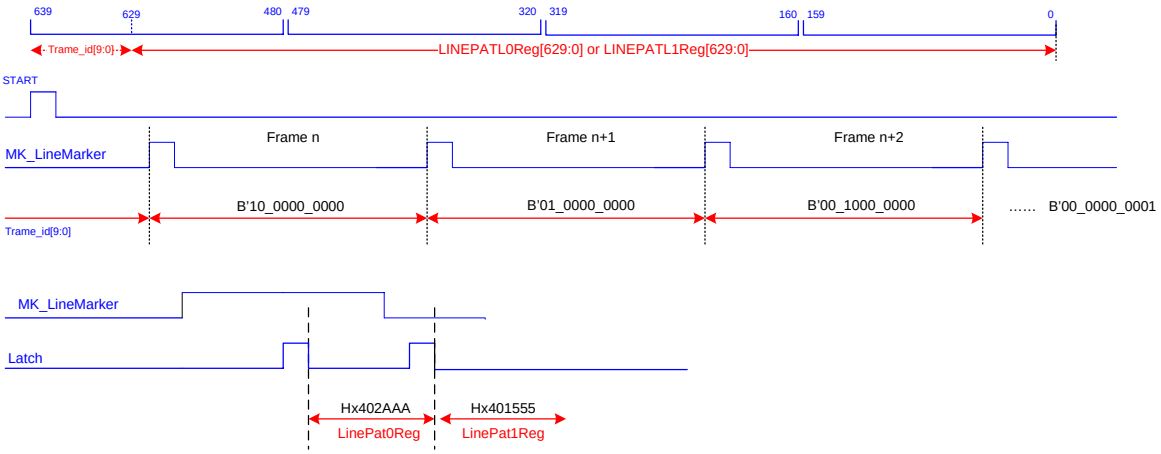


Figure 8 – When *En_LineMarker* is set to 1, the test of the digital data processing is active and 2 additional lines of pre-programmed patterns are added at the end of each frame. Then a new frame begins with the fresh data. Data format of the test-patterns is explained in §2.2.11 and §2.2.12. The frame counter is initialized to 0x200 after *START* and shifted to right at each frame.

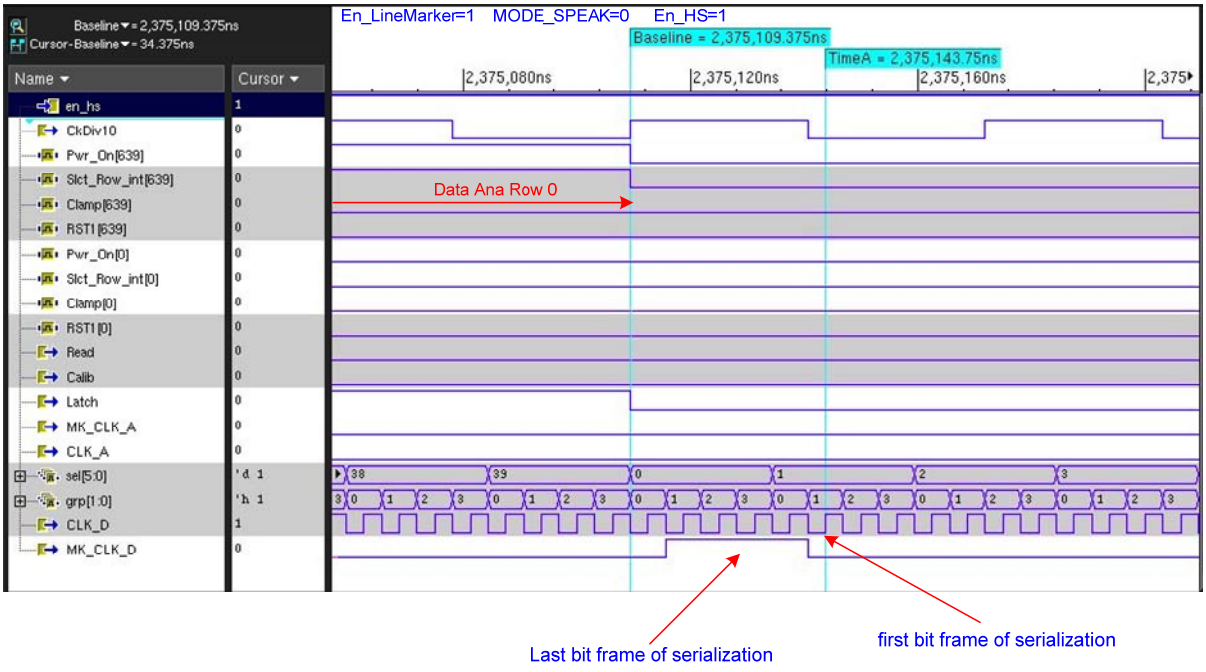


Figure 9 – When En_HS is set to 1, the High Speed mode is activated. The readout clock at 160 MHz comes out from the CLKD pad (or CLK_D internal signal) and a synchronization marker MK_CLK_D appears at the last serialized bit of each frame. This signal is used to sample the first bit of the new frame on the next raising edge of CLKD

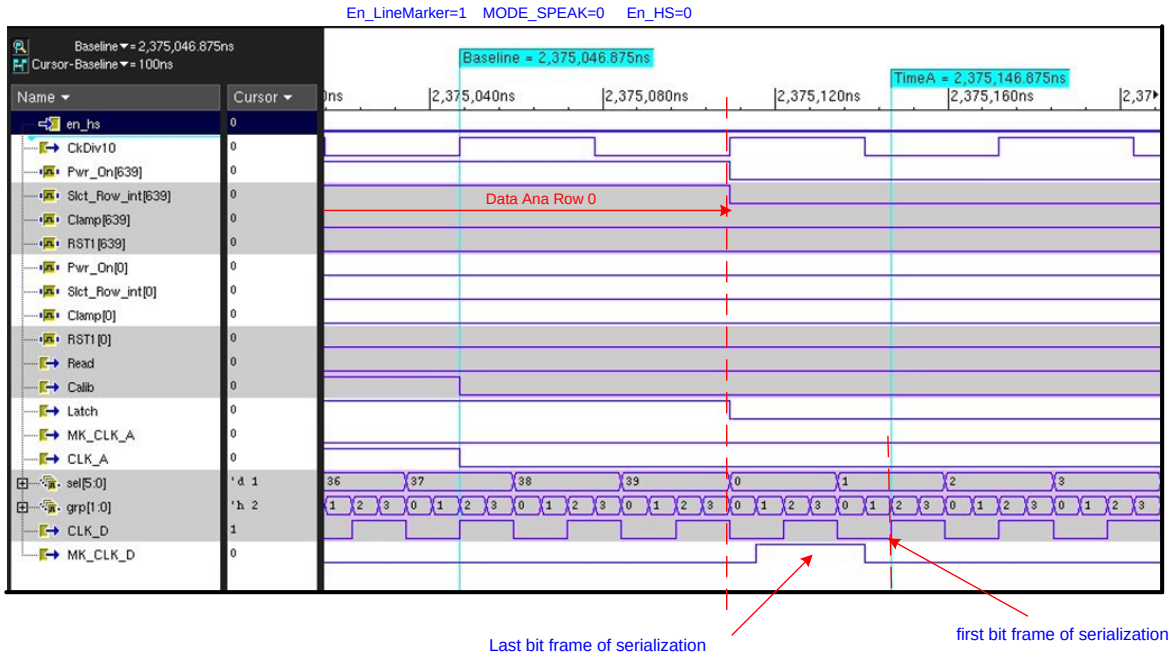


Figure 10 -- When En_HS is set to 0, the Low Speed mode is activated. The readout clock at 40 MHz comes out from the CLKD pad (or CLK_D internal signal) and a synchronization marker MK_CLK_D appears at the last serialized bit of each frame. This signal is used to sample the first bit of the new frame on the next raising edge of CLKD

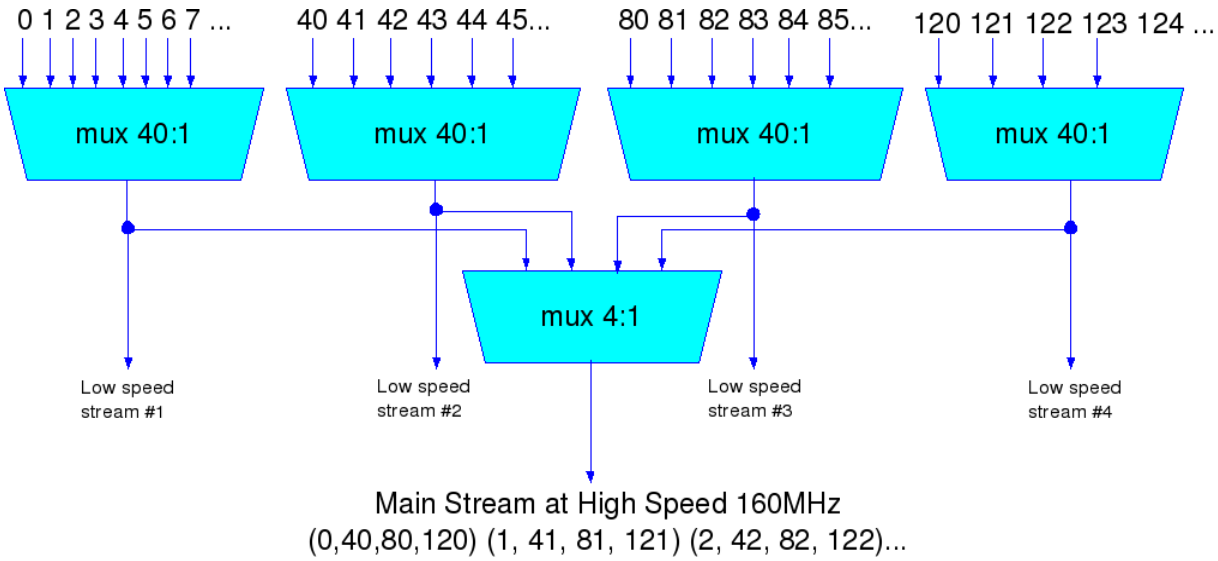


Figure 11 – There are 4 identical serializers in PHASE-1 one for each High Speed output. Here is the basic architecture of one of them which shows the 2 hierarchical levels of multiplexing. The first 40:1 generates the slow speed streams at 40 MHz (only for testing purpose) and the second one 4:1 assembles the data for the High Speed output at 160 MHz. Please observe the sequence at the output: this 2-levels architecture scrambles the data coming out from the high speed output .

3.6.3 Main Signal Specifications

	Parameter	Typical Value	Notes
INIT	RSTB Pulse Width	>1 μS	Active Low, Asynchronous Power on Reset
JTAG	TCK Frequency	10 MHz	Boundary Scan Clock
	TMS Setup/Hold Time	~10 nS	Boundary Scan Control Signal
	TDI Setup/Hold Time	~10 nS	Boundary Scan Serial Data In
READOUT	CKRD Frequency	Up to 100 MHz	Readout Clock LVDS signal
	CKRD Duty Cycle	50%	
	START Setup/Hold Time	5 ns	Chip Initialisation, CMOS signal.
	SPEAK Setup/Hold Time	5 ns	Active Readout Marker & Clock
Analogue Driver	Input Dynamic range		
	Rise time		
	Fall time		
	Bandwidth		
	Output Current Range		

4 Pad Ring

The pad ring of PHASE-1 is build with

- Pads full custom designed for some of the analogue signals and power supplies
- Pads from the AMS library for the digital signals and power supplies

The pad ring is split in 8 functional independent parts

- CMOS JTAG and Test purpose pads
- LVDS Read Out Drivers
- Digital outputs
- Read Out Analogue Outputs
- Bias Test
- Analogue and Digital Power supplies
- Test structure 1
- Test structure 2

Each part has its own supply pads.

4.1 PHASE-1 Pad Ring and Floor Plan View

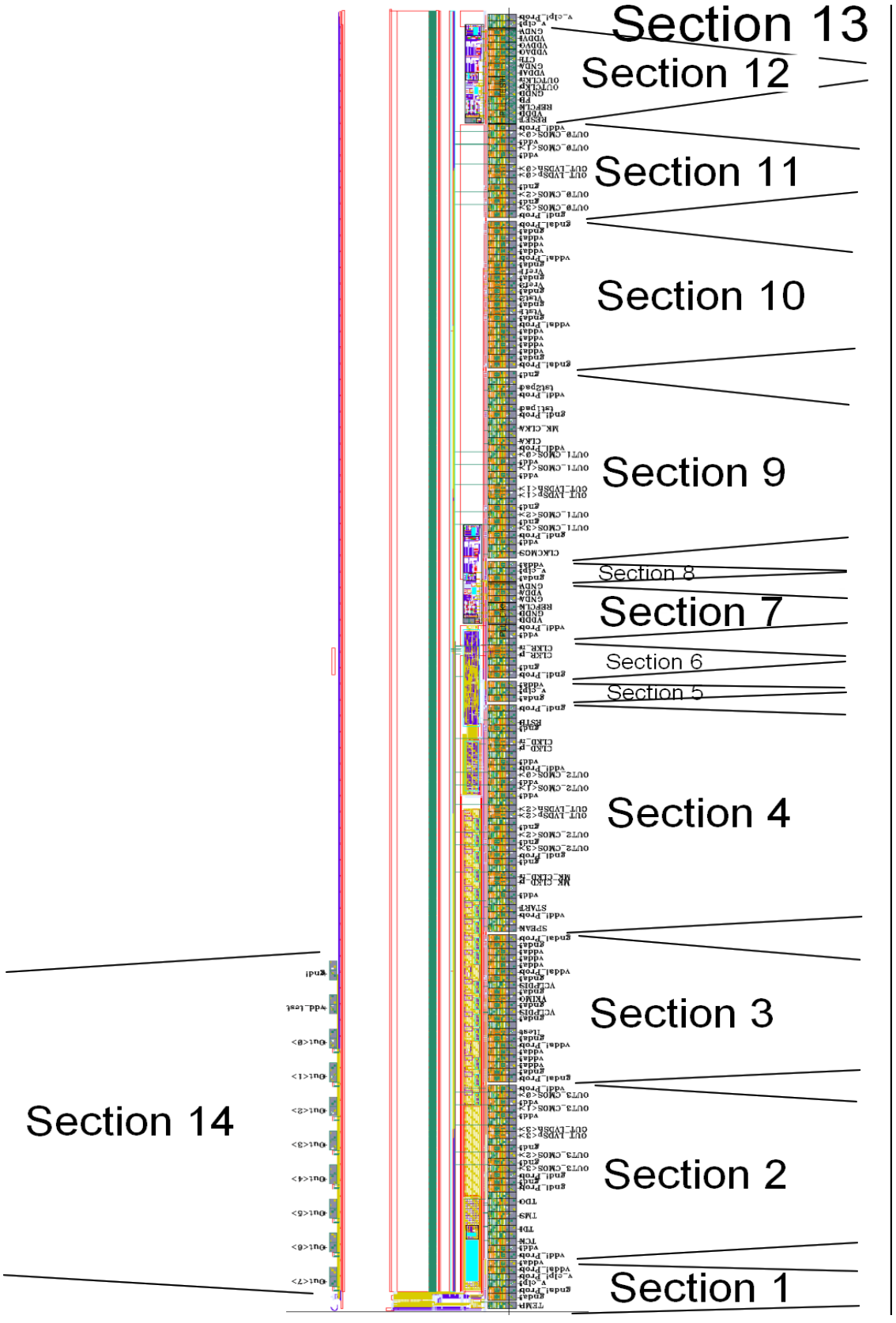


Figure 12 – The pad layout of PHASE-1. Only the top edge and the bottom edge are visible. The pads used for the test with a probe station are also drawn but not named because they reproduce the functionality of the adjacent pad.

4.2 Pad List

Section 1 – Temperature sensor and Analog bias for pixels				
Pad	**Name**	**Description**	**Cell**	**Type**
1	TEMP	temperature sensor	DIRECTPAD	direct pad
2	gnda!	analog ground	AGND3ALLP	power
3	gnda!_Prob (*)	analog ground	AGND3ALLP	power
4	v_clp!	clamping voltage for pixels	DIRECTPAD	power
5	v_clp!_Prob (*)	clamping voltage for pixels	DIRECTPAD	power
6	vdda!_Prob (*)	analog power	AVDD3ALLP	power
7	vdda!	analog power	AVDD3ALLP	power

Section 2 – JTAG control and Digital Output Channel 3				
Pad	**Name**	**Description**	**Cell**	**Type**
8	vdd!_Prob (*)	digital power	VDD3ALLP	power
9	vdd!	digital power	VDD3ALLP	power
10	TCK	JTAG clock	ICCK2P	DI-clockin
---			ProbePad	
11	TDI	JTAG data input	ICUP	DI-pullup
---			ProbePad	
12	TMS	JTAG mode state	ICUP	DI-pullup
---			ProbePad	
13	TDO	JTAG data output	BT4P	DO 3-state, 4mA
---			ProbePad	probe
14	gnd!_Prob (*)	digital ground	GND3ALLP	power
15	gnd!	digital ground	GND3ALLP	power
16	gnd!_Prob (*)	digital ground	GND3ALLP	power
17	OUT3_CMOS<3>	data output slow speed channel 3, stream 3	BU4P	DO 3-state, 4mA
18	gnd!	digital ground	GND3ALLP	power
19	OUT3_CMOS<2>	data output slow speed channel 3, stream 2	BU4P	DO 3-state, 4mA
20	gnd!	digital ground	GND3ALLP	power
---			probePad	probe
21	OUT_LVDSp<3>	data output fast speed, channel 3	LVDS-TX	DO LVDS
22	OUT_LVDSn<3>	data output fast speed, channel 3	LVDS-TX	DO LVDS
---			ProbePad	probe
23	vdd!	digital power	VDD3ALLP	power
24	OUT3_CMOS<1>	data output slow speed channel 3, stream 1	BU4P	DO 3-state, 4mA
25	vdd!	digital power	VDD3ALLP	power
26	OUT3_CMOS<0>	data output slow speed channel 3, stream 0	BU4P	DO 3-state, 4mA
27	vdd!_Prob (*)	digital power	VDD3ALLP	power

Section 3 – Analog bias and DACs

Pad	Name	Description	Cell	Type
28	gnda!_Prob (*)	analog ground	AGND3ALLP	Power
29	gnda!	analog ground	AGND3ALLP	Power
30	vdda!	analog power	AVDD3ALLP	Power
31	vdda!	analog power	AVDD3ALLP	Power
32	vdda!	analog power	AVDD3ALLP	Power
33	vdda!_Prob (*)	analog power	AVDD3ALLP	Power
34	gnda!	analog ground	AGND3ALLP	Power
35	Itest		APRIOP	Power
---			probePad	Probe
36	gnda!	analog ground	AGND3ALLP	Power
37	VCLPDIS	discriminator clamping, external injection	DIRECTPAD	direct pad
38	gnda!	analog ground	AGND3ALLP	Power
39	VKIMO	circuit monitoring	APRIOP	AIO 0 Ohm
40	gnda!	analog ground	AGND3ALLP	Power
41	VCLPDIS	discriminator clamping, external injection	DIRECTPAD	direct pad
42	gnda!	analog ground	AGND3ALLP	Power
43	vdda!_Prob (*)	analog power	AVDD3ALLP	Power
44	vdda!	analog power	AVDD3ALLP	Power
45	vdda!	analog power	AVDD3ALLP	Power
46	vdda!	analog power	AVDD3ALLP	Power
47	gnda!	analog ground	AGND3ALLP	Power
48	gnda!_Prob (*)	analog ground	AGND3ALLP	Power

Section 4 – Synchronization and Digital Output Channel 2				
Pad	**Name**	**Description**	**Cell**	**Type**
49	SPEAK	activate readout marker and clock	ICPD	DI- pulldown
---			probePad	Probe
50	vdd!_Prob (*)	digital power	VDD3ALLP	Power
51	START	synchronize the outputs	ICPD	DI- pulldown
---			probePad	Probe
52	vdd!	digital power	VDD3ALLP	Power
---			probePad	Probe
53	MK_CLKD_p	marker and clock for digital data	LVDS-TX	DO LVDS
54	MK_CLKD_n	marker and clock for digital data	LVDS-TX	DO LVDS
---			probePad	Probe
55	gnd!	digital ground	GND3ALLP	Power
56	gnd!_Prob (*)	digital ground	GND3ALLP	power
57	OUT2_CMOS<3>	data output slow speed channel 2, stream 3	BU4P	DO 3-state, 4mA
58	gnd!	digital ground	GND3ALLP	power
59	OUT2_CMOS<2>	data output slow speed channel 2, stream 2	BU4P	DO 3-state, 4mA
60	gnd!	digital ground	GND3ALLP	power
---			probePad	probe
61	OUT_LVDSp<2>	data output fast speed, channel 2	LVDS-TX	DO LVDS
62	OUT_LVDSn<2>	data output fast speed, channel 2	LVDS-TX	DO LVDS

---			probePad	probe
63	vdd!	digital power	VDD3ALLP	power
64	OUT2_CMOS<1>	data output slow speed channel 2, stream 1	BU4P	DO 3-state, 4mA
65	vdd!	digital power	VDD3ALLP	power
66	OUT2_CMOS<0>	data output slow speed channel 2, stream 0	BU4P	DO 3-state, 4mA
67	vdd!_Prob (*)	digital power	VDD3ALLP	power
68	vdd!	digital power	VDD3ALLP	power
---			probePad	probe
69	CLKD_p	readout clock for digital data	LVDS-TX	DO LVDS
70	CLKD_n	readout clock for digital data	LVDS-TX	DO LVDS
---			probePad	probe
71	gnd!	digital ground		power
72	RSTB	asynchronous reset, active low	ISUP	DI-pullup, schmitt
---			probePad	probe
73	gnd!_Prob (*)	digital ground	GND3ALLP	power

Section 5 – Analog bias for pixels				
Pad	**Name**	**Description**	**Cell**	**Type**
74	gnda!	analog ground	AGND3ALLP	power
75	v_clp!	clamping voltage for pixels	DIRECTPAD	direct pad
76	vdda!	analog power	AVDD3ALLP	power

Section 6 – Master clock (LVDS)				
Pad	**Name**	**Description**	**Cell**	**Type**
77	gnd!_Prob (*)	digital ground	GND3ALLP	power
78	gnd!	digital ground	GND3ALLP	power
---			probePad	probe
79	CKR_p	master clock, LVDS compatible	LVDS-RX	DI LVDS
80	CKR_n	master clock, LVDS compatible	LVDS-RX	DI LVDS
---			probePad	probe
81	vdd!	digital power	VDD3ALLP	power
82	vdd!_Prob (*)	digital power	VDD3ALLP	power

Section 7 – Master clock (PLL synthesizer)				
Pad	**Name**	**Description**	**Cell**	**Type**
83	VDDD	digital power	VDD3ALLP	power
84	GNDD	digital ground	GND3ALLP	power
85	REFCLK	master clock, low frequency	ICCK2P	DI clockin
86	GNDA	analog ground	AGND3ALLP	power
87	VDDA	analog power	AVDD3ALLP	power
88	GNDV	analog ground	AGND3ALLP	power

Section 8 – Analog bias for pixels				
Pad	**Name**	**Description**	**Cell**	**Type**
89	gnda!	analog ground	AGND3ALLP	power
90	v_clp!	clamping voltage for pixels	DIRECTPAD	direct pad

91	vdda!	analog power	AVDD3ALLP	power

Section 9 –Digital Output Channel 1 and Readout clock				
Pad	**Name**	**Description**	**Cell**	**Type**
92	CKCMOS	master clock, CMOS compatible	ICCK2P	DI clockin
---			probePad	probe
93	vdd!	digital power	VDD3ALLP	power
94	gnd!_Prob (*)	digital ground	GND3ALLP	power
95	OUT1_CMOS<3>	data output slow speed channel 1, stream 3	BU4P	DO 3-state, 4mA
96	gnd!	digital ground	GND3ALLP	power
97	OUT1_CMOS<2>	data output slow speed channel 1, stream 2	BU4P	DO 3-state, 4mA
98	gnd!	digital ground	GND3ALLP	power
			probePad	probe
99	OUT_LVDSp<1>	data output fast speed, channel 1	LVDS-TX	DO LVDS
100	OUT_LVDSn<1>	data output fast speed, channel 1	LVDS-TX	DO LVDS
---			ProbePad	probe
101	vdd!	digital power	VDD3ALLP	power
102	OUT1_CMOS<1>	data output slow speed channel 1, stream 1	BU4P	DO 3-state, 4mA
103	vdd!	digital power	VDD3ALLP	power
104	OUT1_CMOS<0>	data output slow speed channel 1, stream 0	BU4P	DO 3-state, 4mA
105	vdd!_Prob (*)	digital power	VDD3ALLP	power
106	CLKA	readout clock for analog data	BT4P	DO 3-state, 4mA
---			probePad	probe
107	MK_CLKA	marker and clock for analog data	BT4P	DO 3-state, 4mA
---			probePad	probe
108	gnda!_Prob (*)	digital ground	GND3ALLP	power
109	tst1pad	readout test pad 1	BT2P	DO 3-state, 2mA
---			probePad	probe
110	vdd!_Prob (*)	digital power	VDD3ALLP	power
111	tst2pad	readout test pad 2	BT2P	DO 3-state, 2mA
---			probePad	probe
112	gnd!	digital ground	GND3ALLP	power

Section 10 – Analog test for discriminator				
Pad	**Name**	**Description**	**Cell**	**Type**
113	gnda!_Prob (*)	analog ground	AGND3ALLP	power
114	gnda!	analog ground	AGND3ALLP	power
115	vdda!	analog power	AVDD3ALLP	power

116	vdda!	analog power	AVDD3ALLP	power
117	vdda!	analog power	AVDD3ALLP	power
118	vdda!	analog power	AVDD3ALLP	power
119	vdda!_Prob (*)	analog power	AVDD3ALLP	power
120	gnda!	analog ground	AGND3ALLP	power
121	Vtst1	vtest1, external injection	APRIOP	AIO 0 Ohm
122	gnda!	analog ground	AGND3ALLP	power
123	Vtst2	vtest2, external injection	APRIOP	AIO 0 Ohm
124	gnda!	analog ground	AGND3ALLP	power
125	Vref2	vref2, external injection	APRIOP	AIO 0 Ohm
126	gnda!	analog ground	AGND3ALLP	power
127	Vref1	vref2, external injection	APRIOP	AIO 0 Ohm
128	gnda!	analog ground	AGND3ALLP	power
129	vdda!_Prob (*)	analog power	AVDD3ALLP	power
130	vdda!	analog power	AVDD3ALLP	power
131	vdda!	analog power	AVDD3ALLP	power
132	vdda!	analog power	AVDD3ALLP	power
133	gnda!	analog ground	AGND3ALLP	power
134	gnda!_Prob (*)	analog ground	AGND3ALLP	power

Section 11 – Digital Output Channel 0				
Pad	**Name**	**Description**	**Cell**	**Type**
135	gnd!_Prob (*)	digital ground	GND3ALLP	power
136	OUT0_CMOS<3>	data output slow speed channel 0, stream 3	BU4P	DO 3-state, 4mA
137	gnd!	digital ground	GND3ALLP	power
138	OUT0_CMOS<2>	data output slow speed channel 0, stream 2	BU4P	DO 3-state, 4mA
139	gnd!	digital ground	GND3ALLP	power
---			probePad	probe
140	OUT_LVDSp<0>	data output fast speed, channel 0	LVDS-TX	DO LVDS
141	OUT_LVDSn<0>	data output fast speed, channel 0	LVDS-TX	DO LVDS
---			ProbePad	probe
142	vdd!	digital power	VDD3ALLP	power
143	OUT0_CMOS<1>	data output slow speed channel 0, stream 1	BU4P	DO 3-state, 4mA
144	vdd!	digital power	VDD3ALLP	power
145	OUT0_CMOS<0>	data output slow speed channel 0, stream 0	BU4P	DO 3-state, 4mA
146	vdd!_Prob (*)	digital power	VDD3ALLP	power

Section 12 – Test: PLL synthesizer				
Pad	**Name**	**Description**	**Cell**	**Type**
147	RESET	asynchronous reset, active low	ISUP	DI-pullup, schmitt

148	VDDD	digital power	VDD3ALLP	power
149	REFCLK	master clock, CMOS compatible	ICCK2P	DI clockin
150	FB	feedback	BU4P	DO 3-state, 4mA
151	GNDD	digital ground	GND3ALLP	power
152	OUTCLOCKp	synthesized clock	LVDS-TX	DO LVDS
153	OUTCLOCKn	synthesized clock	LVDS-TX	DO LVDS
154	VDDAI	analog power	AVDD3ALLP	power
155	GNDA	analog ground	AGND3ALLP	power
156	CTL	voltage control for oscillator	APRIOP	AIO 0 Ohm
157	VDDAO	analog power	AVDD3ALLP	power
158	VDDVO	analog power	AVDD3ALLP	power
159	VDDVI	analog power	AVDD3ALLP	power
160	GNDV	analog ground	AGND3ALLP	power

Section 13 – Analog bias for pixels				
Pad	**Name**	**Description**	**Cell**	**Type**
161	v_clp!	clamping voltage for pixels	DIRECTPAD	direct pad
162	v_clp!_Prob (*)	clamping voltage for pixels	DIRECTPAD	direct pad

Section 14 – Test : Analog outputs from the matrix				
Pad	**Name**	**Description**	**Cell**	**Type**
---			g_pad	test pad
163	gnd!_test	analog ground	g_pad	test pad
---			g_pad	test pad
164	vdda!_test	analog power	g_pad	test pad
---			g_pad	test pad
165	Out<0>	analog output<0> test mode	g_pad	test pad
---			g_pad	test pad
166	Out<1>	analog output<1> test mode	g_pad	test pad
---			g_pad	test pad
167	Out<2>	analog output<2> test mode	g_pad	test pad
---			g_pad	test pad
168	Out<3>	analog output<3> test mode	g_pad	test pad
---			g_pad	test pad
169	Out<4>	analog output<4> test mode	g_pad	test pad
---			g_pad	test pad
170	Out<5>	analog output<5> test mode	g_pad	test pad
---			g_pad	test pad
171	Out<6>	analog output<6> test mode	g_pad	test pad
---			g_pad	test pad
172	Out<7>	analog output<7> test mode	g_pad	test pad

(*) Probe pads are used only for test purpose and should not be bonded